

- ☐ Tentative Specification
☐ Preliminary Specification
☒ Approval Specification

MODEL NO.: V500HK1
 SUFFIX: LS5

Ver. C9

Customer:

APPROVED BY

SIGNATURE

Name / Title

Note

Please return 1 copy for your confirmation with your signature and comments.

Approved By	Checked By	Prepared By
Chao-Chun Chung	Ken Wu	WT Hsu

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REVISION HISTORY

Version	Date	Page (New)	Section	Description
A1	Sep.19,11	all	all	Tentative Specification Ver 0.0 was first issued.
A1	Sep.23,11	48	11	Update MECHANICAL CHARACTERISTIC
B3	Oct 26,11	5	1.1	Update OVERVIEW
		5	1.2	Update FEATURES
		6	1.5	Update MECHANICAL SPECIFICATIONS
		8	2.3.2	Update BACKLIGHT CONVERTER UNIT
		9	3.1	Update TFT LCD MODULE
		12	3.2.1	Update LED LIGHT BARCHARACTERISTICS
		12~13	3.2.2	Update CONVERTER CHARACTERISTICS
		14	3.2.3	Update CONVERTER INTERFACE CHARACTERISTICS
		16	4.1	Update TFT LCD MODULE
		17~19	5.1	Update TFT LCD MODULE
		23~24	5.4	Update BLOCK DIAGRAM OF INTERFACE
		25~26	5.5	Update LVDS INTERFACE
		27	5.6	Update COLOR DATA INPUT ASSIGNMENT
		29~30	6.1	Update INPUT SIGNAL TIMING SPECIFICATIONS
		34	6.2.2	Update 2D/3D MODE CHANGE SIGNAL SEQUENCE WITHOUT VCC TURN OFF AND TURN ON
		35	7.1	Update TEST CONDITIONS
		36、39、41	7.2	Update OPTICAL SPECIFICATIONS
C7	Nov.25,11	9	3.1	Update TFT LCD MODULE
		16	4.1	Update TFT LCD MODULE
		20~21	5.1	Update Note (9)& Note (12) of TFT LCD MODULE
		22	5.2	Update BACKLIGHT UNIT
		29	6.1	Update INPUT SIGNAL TIMING SPECIFICATIONS (Ta = 25 ± 2 °C)
		33	6.1.2	Update Notes(5) of Timing spec for Frame Rate = 60Hz
		35	6.2.2	Update 2D/3D MODE CHANGE SIGNAL SEQUENCE WITHOUT VCC TURN OFF AND TURN ON
		36	7.1	Update TEST CONDITIONS
		37	7.2	Update OPTICAL SPECIFICATIONS & Notes(4) 、 (5) 、 (6) 、 (8)
		44	9.1	Update PACKING SPECIFICATIONS
		47~48	11	Update MECHANICAL CHARACTERISTIC

C7	Dec.21	1	1.1	Update OVERVIEW
		1	1.2	Update FEATURES
		17	4.1	Update TFT LCD MODULE
		18~19	5.1	Update TFT LCD MODULE
		29~33	6.1	Update INPUT SIGNAL TIMING SPECIFICATIONS
		35	6.2.2	Update 2D/3D MODE CHANGE SIGNAL SEQUENCE WITHOUT VCC TURN OFF AND TURN ON
		49		Update Appendix A
C8	Jan.6	13	3.2.1	Update LED LIGHT BAR CHARACTERISTICS
		13~14	3.2.2	Update CONVERTER CHARACTERISTICS
		16	3.2.3	Update CONVERTER INTERFACE CHARACTERISTICS Fig. 2
		37	7.2	Update OPTICAL SPECIFICATIONS
		44~45	9.2	Update PACKING METHOD
		47~48	11	Update MECHANICAL CHARACTERISTIC
C8	May 16	11	3.1	Update TFT LCD MODULE
C9	Jun 20	39	7.2	Update OPTICAL SPECIFICATIONS
		47	9.2	Update PACKAGING METHOD

1. GENERAL DESCRIPTION

1.1 OVERVIEW

V500HK1-LS5 is a 50" TFT Liquid Crystal Display module with LED Backlight unit and 2ch-LVDS interface. This module supports 1920 x 1080 HDTV format and can display true 16.7M colors (8-bits color). The driving board module for backlight is built-in.

1.2 FEATURES

- High brightness 350nits
- High contrast ratio 5000:1
- Fast response time Gray to Gray typical 6.5ms
- High color saturation 72% NTSC
- Full HDTV (1920 x 1080 pixels) resolution, true HDTV format
- LVDS (Low Voltage Differential Signaling) interface
- Optimized response time for 120 Hz frame rate
- Ultra wide viewing angle: Super MVA technology
- RoHs compliance
- T-con input frame rate: 50Hz/60Hz, output frame rate: 100Hz/120Hz

1.3 APPLICATION

- Standard Living Room TVs.
- Public Display Application.
- Home Theater Application.
- MFM Application.

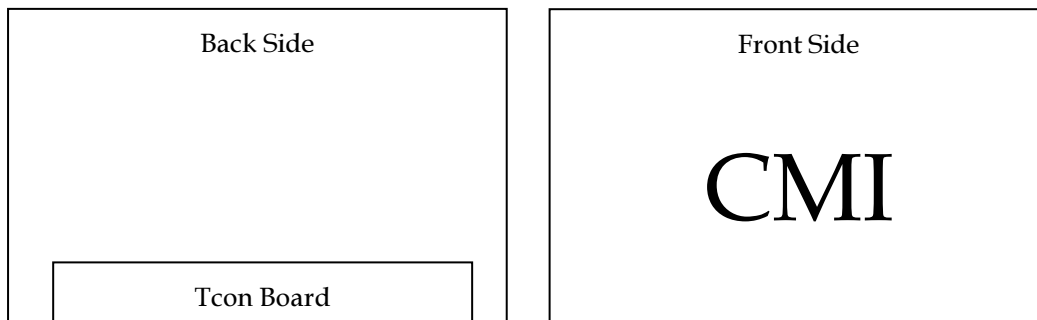
1.4 GENERAL SPECIFICATIONS

Item	Specification	Unit	Note
Active Area	1095.84(H) x (V) 616.41 (50" diagonal)	mm	(1)
Bezel Opening Area	1102.84(H) x 623.41(V)	mm	
Driver Element	a-si TFT active matrix	-	-
Pixel Number	1920 x R.G.B. x 1080	pixel	-
Pixel Pitch(Sub Pixel)	0.1903(H) x 0.5708(V)	mm	-
Pixel Arrangement	RGB vertical stripe	-	-
Display Colors	16.7M	color	-
Display Operation Mode	Transmissive mode / Normally black	-	-
Surface Treatment	Anti-Glare coating (3.5% Low Haze)	-	(2)
Rotation Function	Unachievable		(3)
Display Orientation	Signal input with "CMI"		(3)

Note (1) Please refer to the attached drawings in chapter 9 for more information about the front and back outlines.

Note (2) The spec of the surface treatment is temporarily for this phase. CMI reserves the rights to change this feature.

Note (3)



1.5 MECHANICAL SPECIFICATIONS

Item		Min.	Typ.	Max.	Unit	Note
Module Size Weight	Horizontal (H)	1121.14	1122.64	1124.14	mm	Module Size
	Vertical (V)	643.81	645.31	646.81	mm	
	Depth (D)	14.1	15.1	16.1	mm	To Rear
		23	24	25	mm	To converter cover
	Weight		14000		Kg	Weight

Note (1) Please refer to the attached drawings for more information of front and back outline dimensions.

Note (2) Module Depth does not include connectors.

2. ABSOLUTE MAXIMUM RATINGS

2.1 ABSOLUTE RATINGS OF ENVIRONMENT

Item	Symbol	Value		Unit	Note
		Min.	Max.		
Storage Temperature	T _{ST}	-20	+60	°C	(1)
Operating Ambient Temperature	T _{OP}	0	50	°C	(1), (2)
Shock (Non-Operating)	S _{NOP}	-	35	G	(3), (5)
Vibration (Non-Operating)	V _{NOP}	-	1.0	G	(4), (5)

Note (1) Temperature and relative humidity range is shown in the figure below.

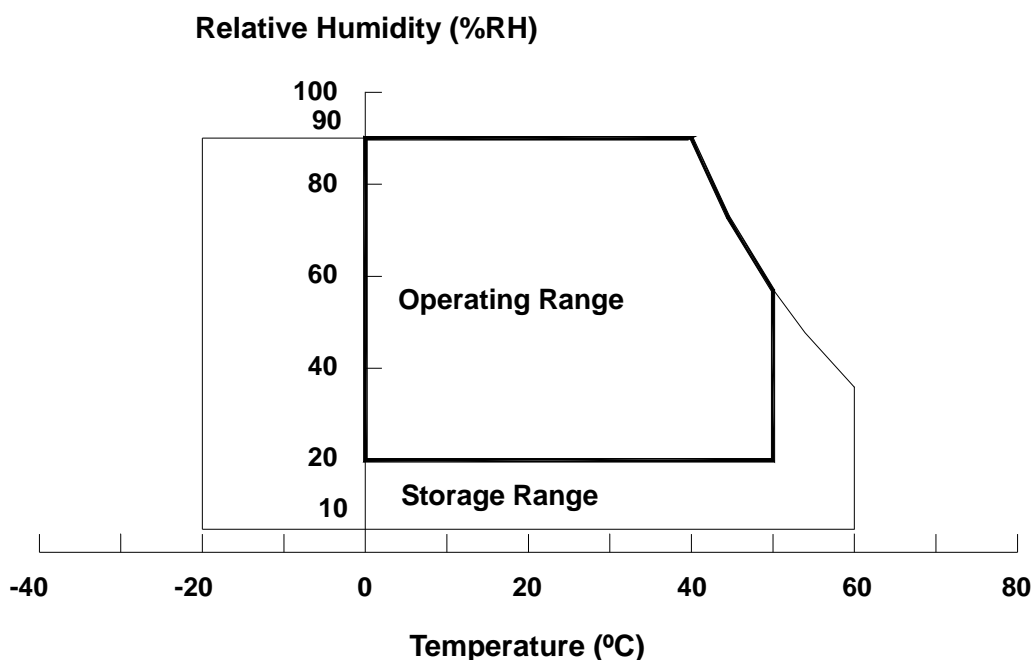
- (a) 90 %RH Max. ($T_a \leq 40$ °C).
- (b) Wet-bulb temperature should be 39 °C Max. ($T_a > 40$ °C).
- (c) No condensation.

Note (2) The maximum operating temperature is based on the test condition that the surface temperature of display area is less than or equal to 65 °C with LCD module alone in a temperature controlled chamber. Thermal management should be considered in final product design to prevent the surface temperature of display area from being over 65 °C. The range of operating temperature may degrade in case of improper thermal management in final product design.

Note (3) 11 ms, half sine wave, 1 time for $\pm X$, $\pm Y$, $\pm Z$.

Note (4) 10 ~ 200 Hz, 30 min, 1 time each X, Y, Z.

Note (5) At testing Vibration and Shock, the fixture in holding the module has to be hard and rigid enough so that the module would not be twisted or bent by the fixture.



2.2 PACKAGE STORAGE

When storing modules as spares for a long time, the following precaution is necessary.

- (a) Do not leave the module in high temperature, and high humidity for a long time, It is highly recommended to store the module with temperature from 0 to 35 °C at normal humidity without condensation.
- (b) The module shall be stored in dark place. Do not store the TFT-LCD module in direct sunlight or fluorescent light.

2.3 ELECTRICAL ABSOLUTE RATINGS

2.3.1 TFT LCD MODULE

Item	Symbol	Value		Unit	Note
		Min.	Max.		
Power Supply Voltage	V _{CC}	-0.3	13.5	V	(1)
Logic Input Voltage	V _{IN}	-0.3	3.6	V	

2.3.2 BACKLIGHT CONVERTER UNIT

Item	Symbol	Test Condition	Min.	Type	Max.	Unit	Note
Light Bar Voltage	V _W	Ta = 25 °C	-	-	60	V _{RMS}	3D Mode
Converter Input Voltage	V _{BL}	-	0	-	30	V	
Control Signal Level	-	-	-0.3	-	6	V	

Note (1) Permanent damage to the device may occur if maximum values are exceeded. Function operation should be restricted to the conditions described under Normal Operating Conditions.

Note (2) No moisture condensation or freezing.

Note (3) The control signals include On/Off Control and External PWM Control.

3. ELECTRICAL CHARACTERISTICS

3.1 TFT LCD MODULE

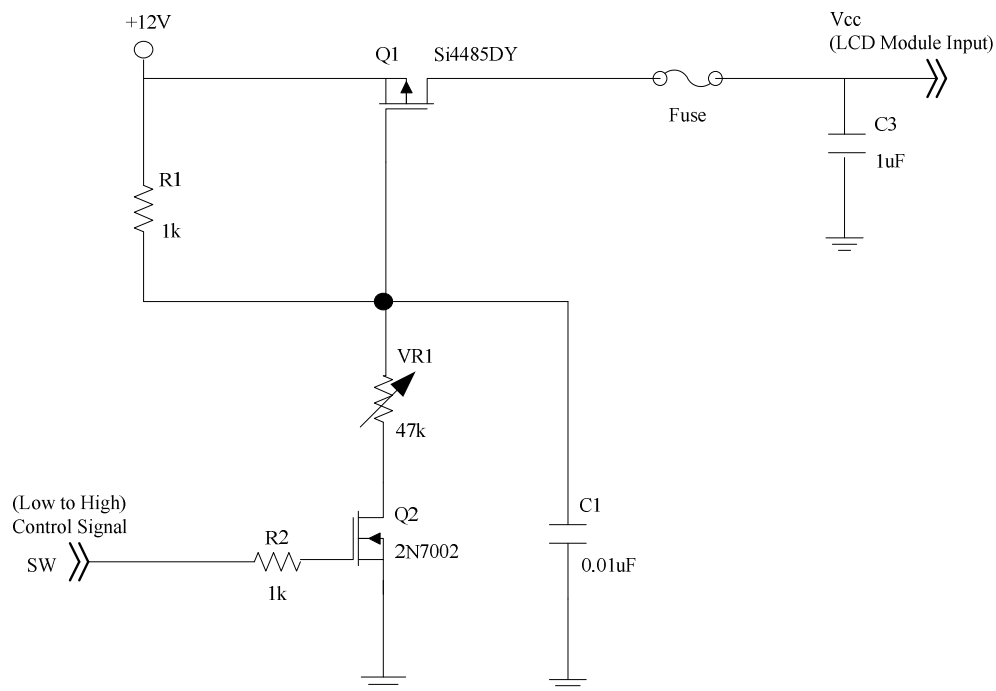
(Ta = 25 ± 2 °C)

Parameter		Symbol	Value			Unit	Note
			Min.	Typ.	Max.		
Power Supply Voltage		V _{CC}	10.8	12	13.2	V	(1)
Rush Current		I _{RUSH}	—	—	3.06	A	(2)
Power Consumption	White Pattern	P _T	—	7.2	8.6	W	(3)
	Horizontal Stripe	P _T	—	15.8	19.0	W	
	Black Pattern	P _T	—	7.3	8.7	W	
Power Supply Current	White Pattern	—	—	0.6	0.72	A	
	Horizontal Stripe	—	—	1.3	1.6	A	
	Black Pattern	—	—	0.61	0.73	A	
LVDS interface	Differential Input High Threshold Voltage	V _{LVTH}	+100	—	+300	mV	(4)
	Differential Input Low Threshold Voltage	V _{LVTL}	-300	—	-100	mV	
	Common Input Voltage	V _{CM}	1.0	1.2	1.4	V	
	Differential input voltage (single-end)	V _{ID}	200	—	600	mV	
	Terminating Resistor	R _T	—	100	—	ohm	
CMIS interface	Input High Threshold Voltage	V _{IH}	2.7	—	3.3	V	
	Input Low Threshold Voltage	V _{IL}	0	—	0.7	V	

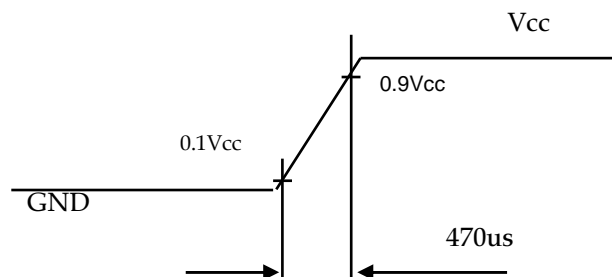
Note (1) The module should be always operated within the above ranges.

The ripple voltage should be controlled under 10% of V_{CC} (Typ.)

Note (2) Measurement condition:



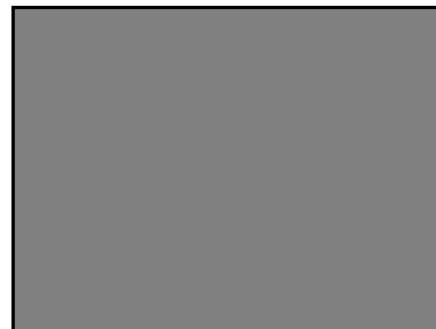
Vcc rising time is 470us



Note (3) The specified power consumption and power supply current is under the conditions at $V_{cc} = 12\text{ V}$, $T_a = 25 \pm 2\text{ }^{\circ}\text{C}$, $f_v = 120\text{ Hz}$, whereas a power dissipation check pattern below is displayed.

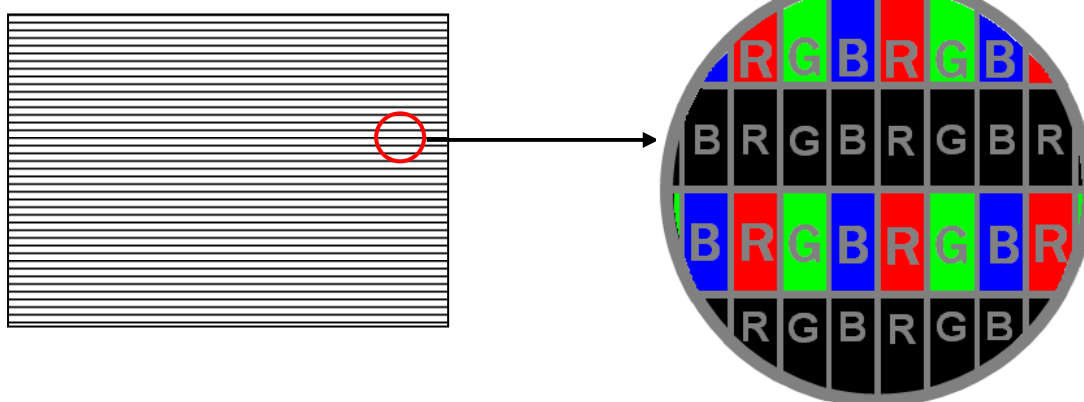
a. White Pattern

b. Black Pattern

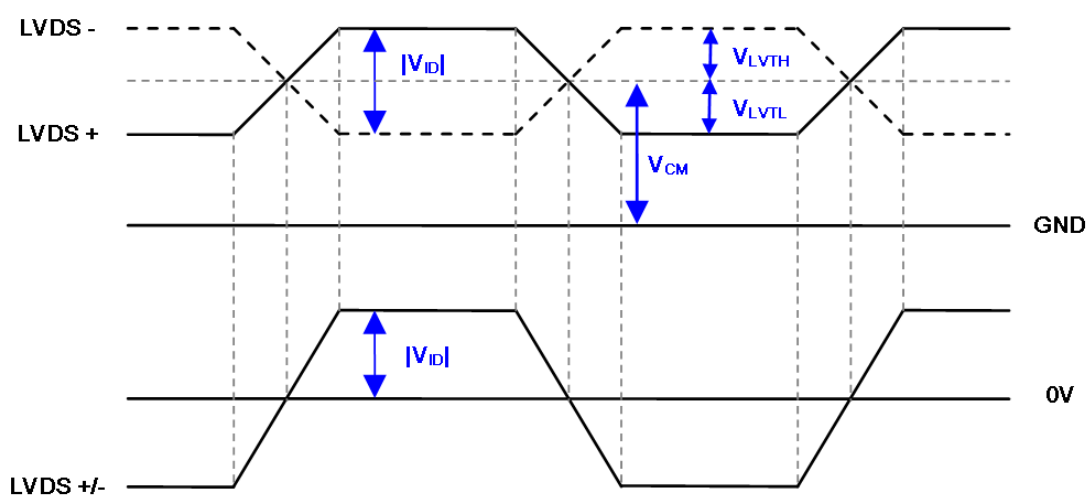


Active Area

c. Horizontal Pattern



Note (4) The LVDS input characteristics are as follows:



3.2 BACKLIGHT UNIT

3.2.1 LED LIGHT BARCHARACTERISTICS (Ta = 25 ± 2 °C)

Parameter	Symbol	Value	Unit	Note
-----------	--------	-------	------	------

		Min.	Typ.	Max.		
Total Current (16 String)	If	-	1840	1952	mA	
One String Current	I _{L(2D)}	-	115	122	mA	
	I _{L(3D)}	-	400	424	mA _{peak}	3D ENA=ON
LED Forward Voltage	V _f	5.5	6.15	7	V _{DC}	I _L =115mA
One String Voltage	V _W	44	-	56	V _{DC}	I _L =115mA
One String Voltage Variation	ΔV _W	-	-	2	V	
Life time	-	30,000	-	-	Hrs	(1)

Note (1) The lifetime is defined as the time which luminance of the LED decays to 50% compared to the initial value, Operating condition: Continuous operating at Ta = 25±2°C, I_L =115mA.

3.2.2 CONVERTER CHARACTERISTICS (Ta = 25 ± 2 °C)

Parameter	Symbol	Value			Unit	Note
		Min.	Typ.	Max.		
Power Consumption	P _{BL(2D)}	-	87.3	100.4	W	(1), (2) IL = 115mA
	P _{BL(3D)}	-	85	96	W	(1), (2) IL=400mA.
Converter Input Voltage	VBL	22.8	24.0	25.2	VDC	
Converter Input Current	I _{BL(2D)}	—	3.64	4.2	A	Non Dimming
	I _{BL(3D)}	—	3.54	4	A	
Input Inrush Current	I _{R(2D)}	-	-	6.5	A _{peak}	V _{BL} =22.8V,(IL=typ.) (3), (6)
	I _{R(3D)}	-	-	10	A _{peak}	V _{BL} =22.8V,(IL= 360mA.)(3), (6)
Dimming Frequency	FB	170	180	190	Hz	(5)
Dimming Duty Ratio	DDR	5	-	100	%	(4), (5)

Note (1) The power supply capacity should be higher than the total converter power consumption P_{BL}. Since the pulse width modulation (PWM) mode was applied for backlight dimming, the driving current changed as PWM duty on and off. The transient response of power supply should be considered for the changing loading when converter dimming.

Note (2) The measurement condition of Max. value is based on 50" backlight unit under input voltage 24V, average LED current 122 mA at 2D Mode (LED current 424 mA_{peak} at 3D Mode) and lighting 1 hour later.

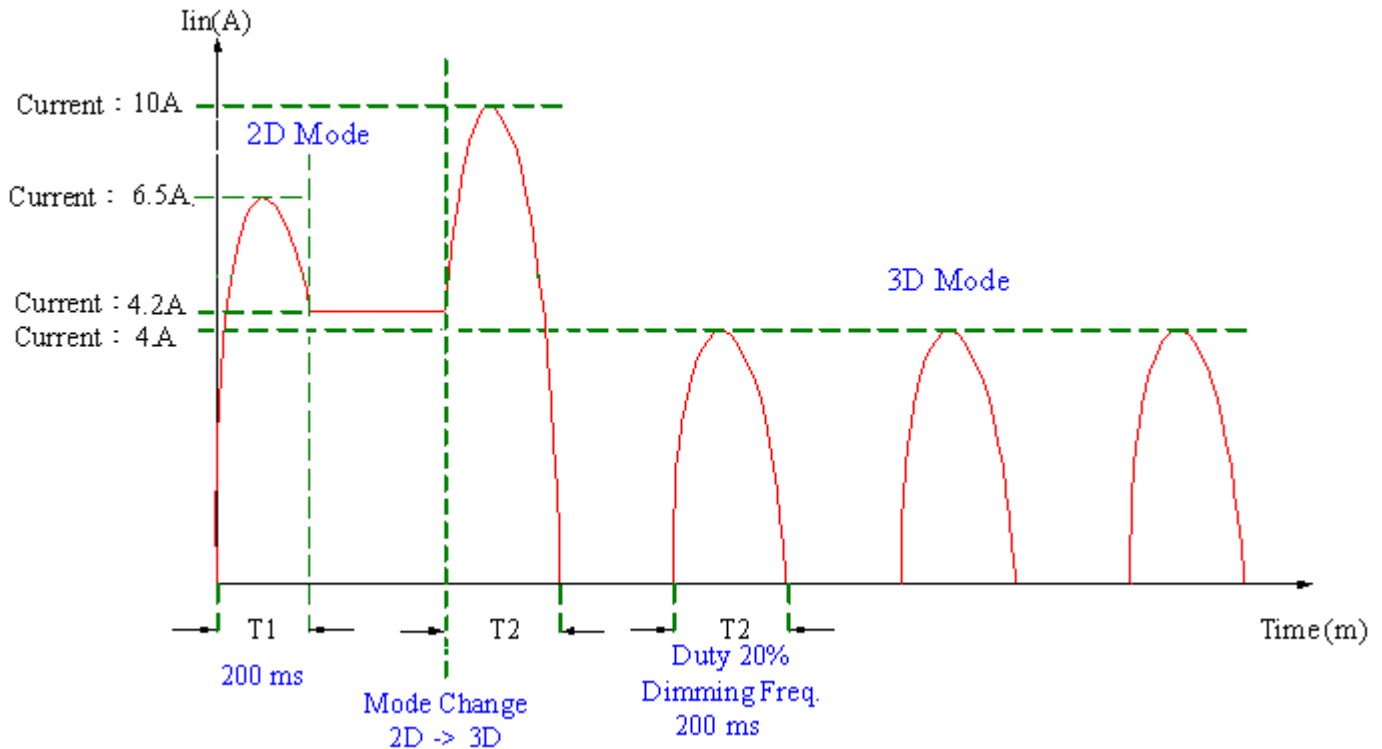
Note (3) For input inrush current measure, the VBL rising time from 10% to 90% is about 30ms.

Note (4) EPWM signal have to input available duty range. Between 97% and 100% duty(DDR) have to be avoided. ($97\% < \text{DDR} < 100\%$) But 100% duty(DDR) is possible. 5% duty(DDR) is only valid for electrical operation.

Note (5) FB and DDR are available only at 2D Mode.

Note (6) Below diagram is only for power supply design reference.

Test Condition: $V_{BL}=22.8V, I_L=115mA$ at 2D Mode/ $I_L=(400)mA$ peak at 3D Mode.



3.2.3 CONVERTER INTERFACE CHARACTERISTICS

Parameter	Symbol	Test Condition	Value			Unit	Note
			Min.	Typ.	Max.		

On/Off Control Voltage	ON	VBLON	—	2.0	—	5.0	V		
	OFF		—	0	—	0.8	V		
External PWM Control Voltage	HI	VEPWM	—	2.0	—	5.25	V	Duty on	(5), (6)
	LO		—	0	—	0.8	V	Duty off	
External PWM Frequency		F _{EPWM}	—	150	160	170	Hz	Normal mode (7)	
Error Signal		ERR	—	—	—	—	—	Abnormal: Open collector Normal: GND (4)	
VBL Rising Time		Tr1	—	20	—	—	ms	10%-90%V _{BL}	
Control Signal Rising Time		Tr	—	—	—	100	ms		
Control Signal Falling Time		Tf	—	—	—	100	ms		
PWM Signal Rising Time		TPWMR	—	—	—	50	us	(6)	
PWM Signal Falling Time		TPWMF	—	—	—	50	us		
Input Impedance		Rin	—	1	—	—	MΩ	EPWM, BLON	
PWM Delay Time		TPWM	—	100	—	—	ms	(6)	
BLON Delay Time	T _{on}		—	300	—	—	ms		
	T _{on1}		—	300	—	—	ms		
BLON Off Time		Toff	—	300	—	—	ms		

Note (1) The Dimming signal should be valid before backlight turns on by BLON signal. It is inhibited to change the external PWM signal during backlight turn on period.

Note (2) The power sequence and control signal timing are shown in the Fig.1. For a certain reason, the converter has a possibility to be damaged with wrong power sequence and control signal timing.

Note (3) While system is turned ON or OFF, the power sequences must follow as below descriptions:

Turn ON sequence: VBL → PWM signal → BLON

Turn OFF sequence: BLOFF → PWM signal → VBL

Note (4) When converter protective function is triggered, ERR will output open collector status. Please refers to Fig.2.

Note (5) The EPWM interface that inserts a pull up resistor to 5V in Max Duty (100%), please refers to Fig.3.

Note (6) EPWM is available only at 2D Mode.

Note (7) EPWM signal have to input available frequency range.

Note (8) [Recommend] EPWM duty ratio is set at 100%(Max. Brightness) in 3D Mode.

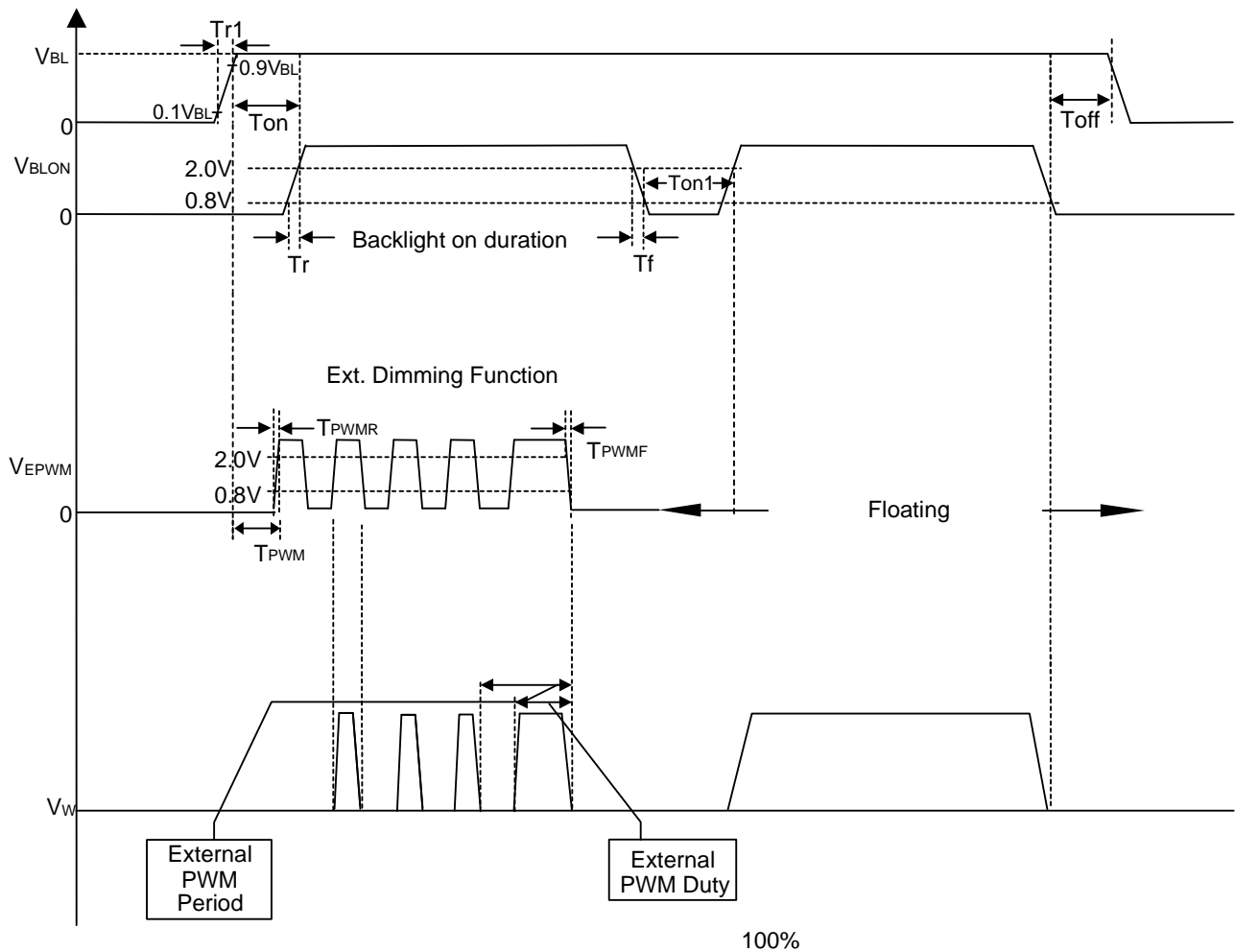


Fig. 1

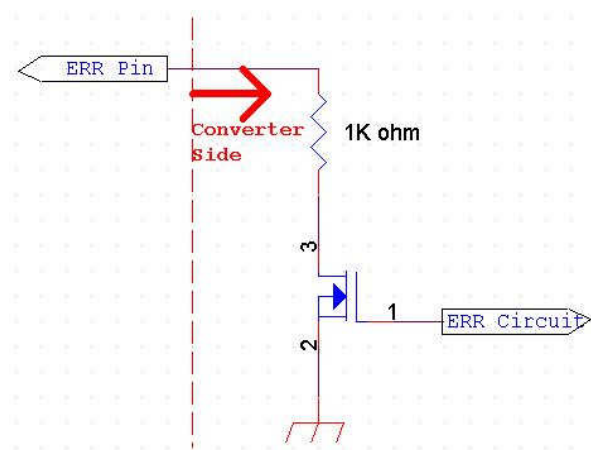


Fig. 2

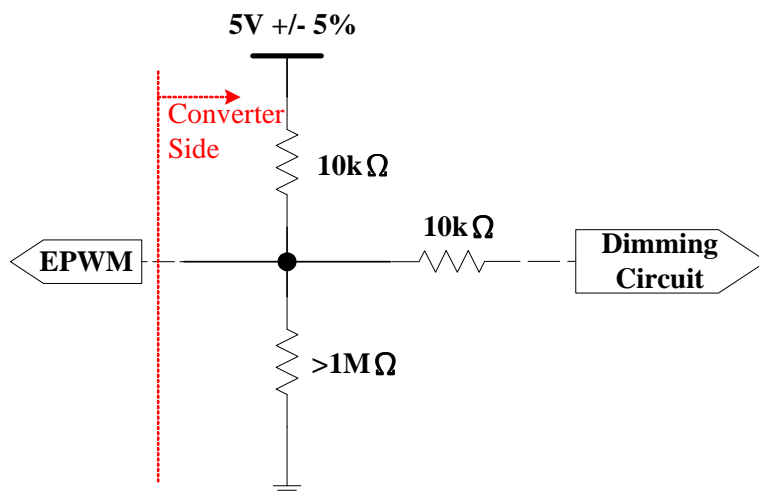
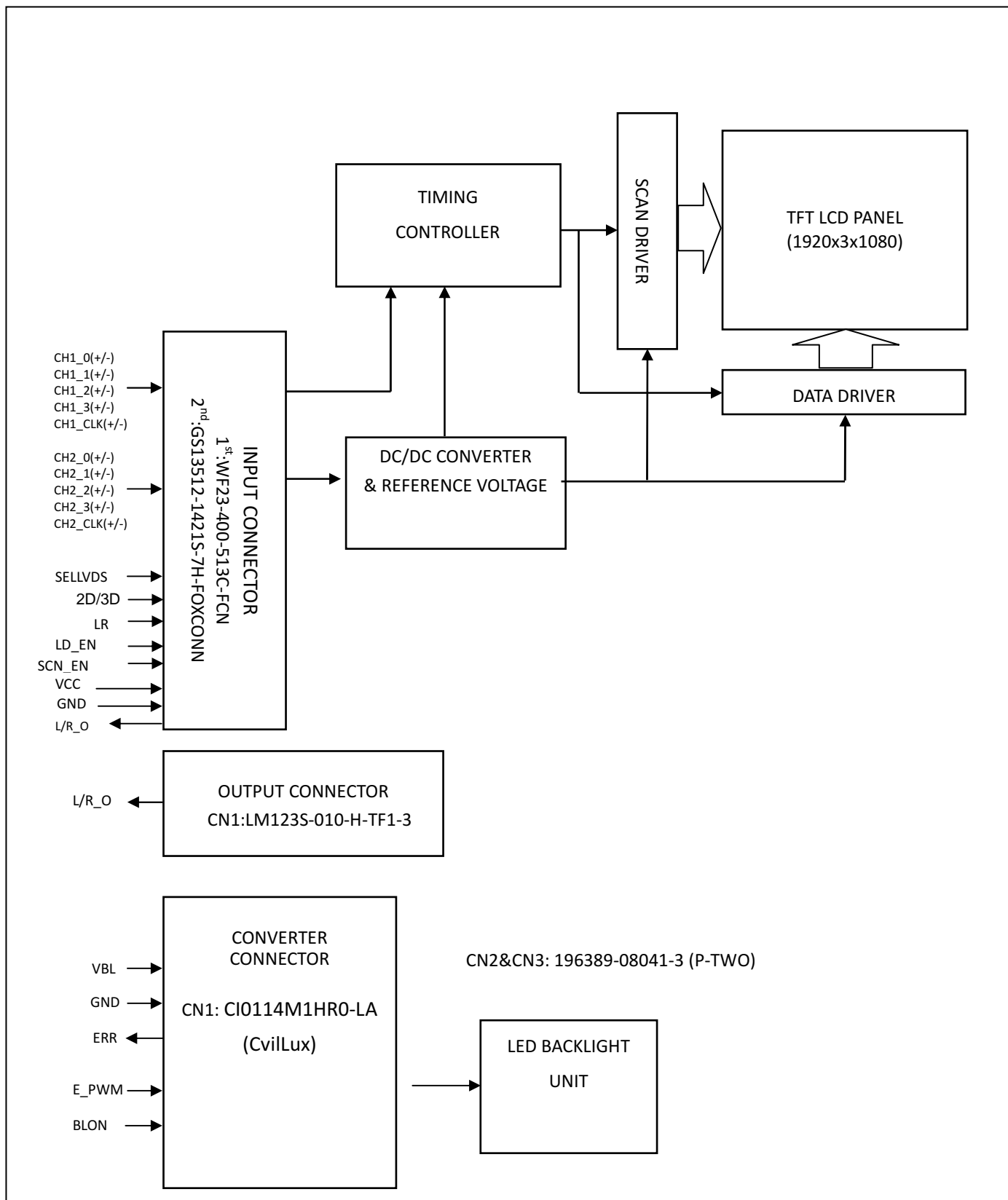


Fig. 3

4. BLOCK DIAGRAM OF INTERFACE

4.1 TFT LCD MODULE



5 .INPUT TERMINAL PIN ASSIGNMENT

5.1 TFT LCD MODULE

CNF1 Connector Part No.: FCN (WF23-400-513C)

Pin	Name	Description	Note
1	N.C.	No Connection	(1)
2	SCL	I2C Serial Clock (for 3D format selection function)	(11)
3	SDA	I2C Serial Data (for 3D format selection function)	
4	N.C.	No Connection	(1)
5	L/R_O	Output signal for Left Right Glasses control	(10)
6	N.C.	No Connection	(1)
7	SELLVDS	Input signal for LVDS Data Format Selection	(2)(7)
8	N.C.	No Connection	(1)
9	N.C.	No Connection	
10	N.C.	No Connection	
11	GND	Ground	
12	ORX0-	Odd pixel Negative LVDS differential data input. Channel 0	(9)
13	ORX0+	Odd pixel Positive LVDS differential data input. Channel 0	
14	ORX1-	Odd pixel Negative LVDS differential data input. Channel 1	
15	ORX1+	Odd pixel Positive LVDS differential data input. Channel 1	
16	ORX2-	Odd pixel Negative LVDS differential data input. Channel 2	
17	ORX2+	Odd pixel Positive LVDS differential data input. Channel 2	
18	GND	Ground	
19	OCLK-	Odd pixel Negative LVDS differential clock input	(9)
20	OCLK+	Odd pixel Positive LVDS differential clock input	
21	GND	Ground	
22	ORX3-	Odd pixel Negative LVDS differential data input. Channel 3	(9)
23	ORX3+	Odd pixel Positive LVDS differential data input. Channel 3	
24	N.C.	No Connection	(1)
25	N.C.	No Connection	
26	2D/3D	Input signal for 2D/3D Mode Selection	(3)(6)(8)
27	L/R	Input signal for Left Right eye frame synchronous(Frame sequence mode)	(4)(8)

28	ERX0-	Even pixel Negative LVDS differential data input. Channel 0	(9)
29	ERX0+	Even pixel Positive LVDS differential data input. Channel 0	
30	ERX1-	Even pixel Negative LVDS differential data input. Channel 1	
31	ERX1+	Even pixel Positive LVDS differential data input. Channel 1	
32	ERX2-	Even pixel Negative LVDS differential data input. Channel 2	
33	ERX2+	Even pixel Positive LVDS differential data input. Channel 2	
34	GND	Ground	
35	ECLK-	Even pixel Negative LVDS differential clock input.	(9)
36	ECLK+	Even pixel Positive LVDS differential clock input.	
37	GND	Ground	
38	ERX3-	Even pixel Negative LVDS differential data input. Channel 3	(9)
39	ERX3+	Even pixel Positive LVDS differential data input. Channel 3	
40	N.C.	No Connection	(1)
41	N.C.	No Connection	
42	LD_EN	Input signal for Local Dimming Enable	(5)(8)
43	SCN_EN	Input signal for Scanning Enable	(6)(8)
44	GND	Ground	
45	GND	Ground	
46	GND	Ground	
47	N.C.	No Connection	(1)
48	VCC	+12V power supply	
49	VCC	+12V power supply	
50	VCC	+12V power supply	
51	VCC	+12V power supply	

CN1 Connector Pin Assignment LM123S-010-H-TF1-3 (UNE)

1	N.C.	No Connection	(1)
2	N.C.	No Connection	
3	N.C.	No Connection	
4	GND	Ground	
5	N.C.	No Connection	(1)
6	L/R_O	Output signal for Left Right Glasses control	(10)
7	N.C.	No Connection	(1)
8	N.C.	No Connection	
9	N.C.	No Connection	
10	N.C.	No Connection	

Note (1) Reserved for internal use. Please leave it open.

Note (2) LVDS format selection.

L= Connect to GND, H=Connect to +3.3V or Open

SELLVDS	Note
L	JEIDA Format
H or Open	VESA Format

Note (3) 2D/3D mode selection.

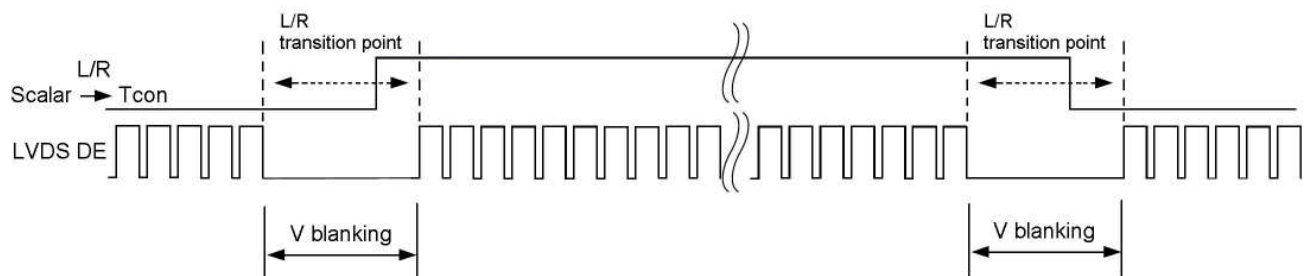
L= Connect to GND or Open, H=Connect to +3.3V

2D/3D	Note
L or Open	2D Mode
H	3D Mode

Note (4) Input signal for Left Right eye frame synchronous

$V_{IL}=0\sim 0.8\text{ V}$, $V_{IH}=2.0\sim 3.3\text{ V}$

L/R	Note
L	Right synchronous signal
H	Left synchronous signal



Note (5) Local dimming enable selection.

L= Connect to GND, H=Connect to +3.3V or Open

LD_EN	Note
L	Local Dimming Disable
H or Open	Local Dimming Enable

LD_EN enable pin should be set in power on stage.

Backlight should be turned off in the period of changing original setting after power on.

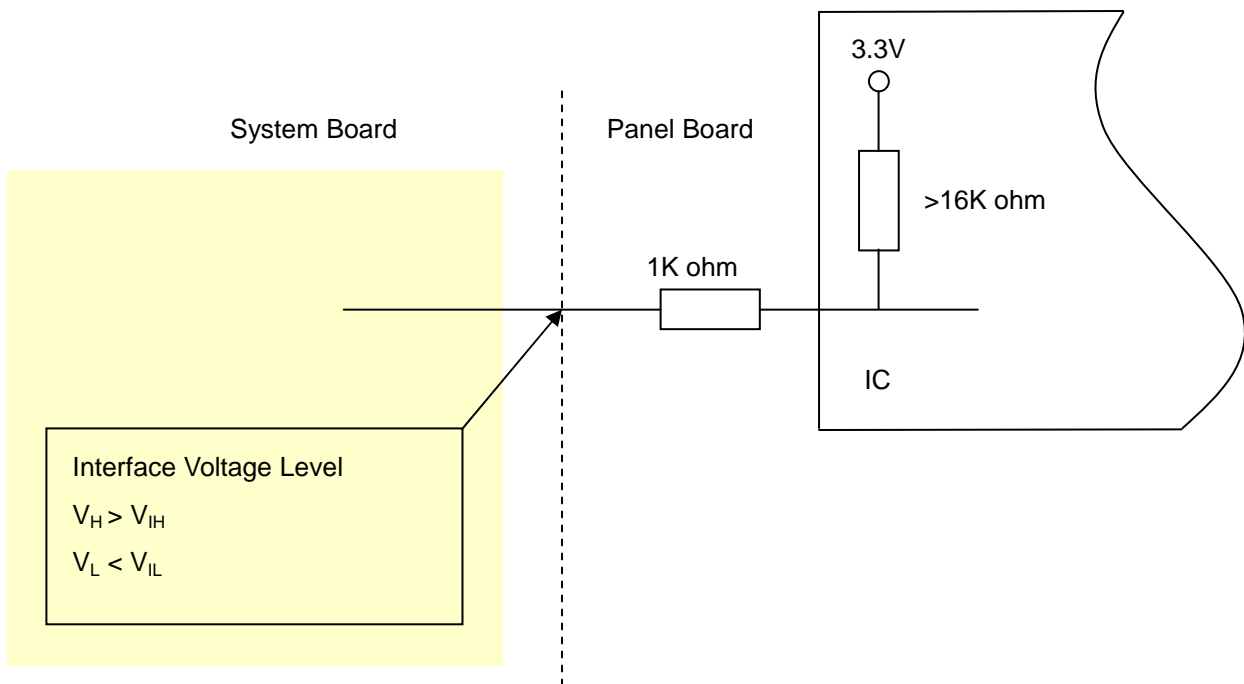
Note (6) Scanning enable selection.

L= Connect to GND or Open, H=Connect to +3.3V

SCN_EN	Note
L or Open	Scanning Disable
H	Scanning Enable

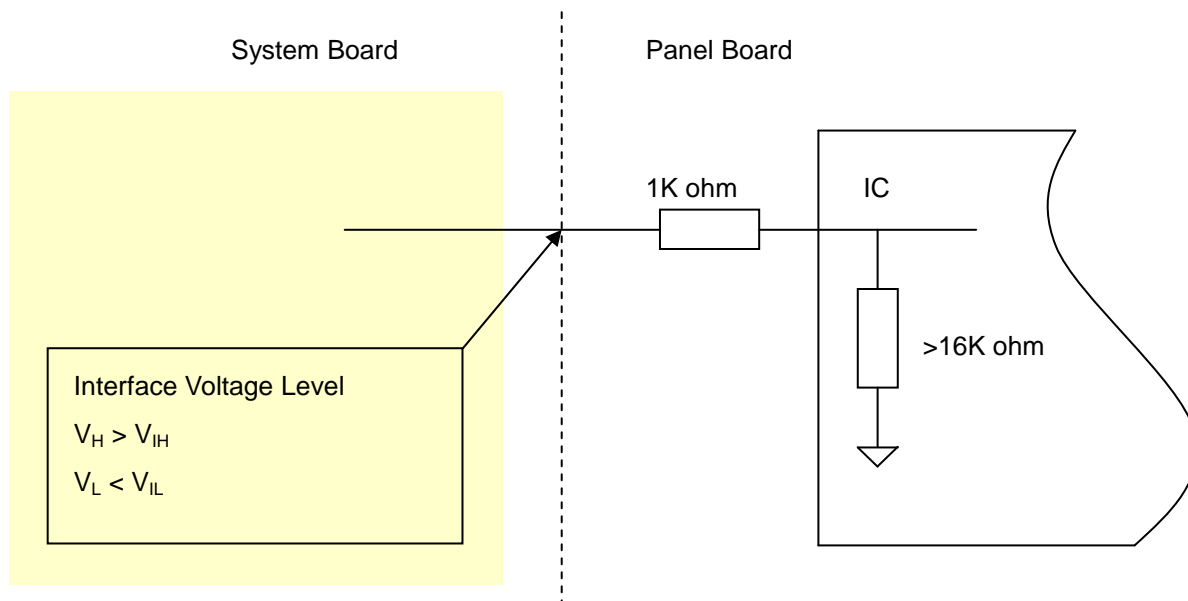
Note (7) Interface optional pin has internal scheme as following diagram.

Customer should keep the interface voltage level requirement which including Panel board loading as below.



Note (8) Interface optional pin has internal scheme as following diagram.

Customer should keep the interface voltage level requirement which including Panel board loading as below.



Note (9) Two pixel data send into the module for every clock cycle. The first pixel of the frame is odd pixel and the second pixel is even pixel.

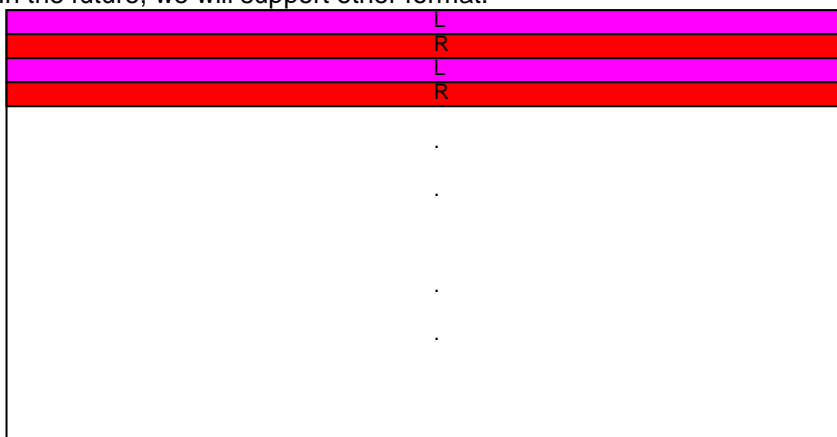
Note (10) The definition of L/R_O signal as follows

L= 0V , H= +3.3V

L/R_O	Note
L	Right glass turn on
H	Left glass turn on

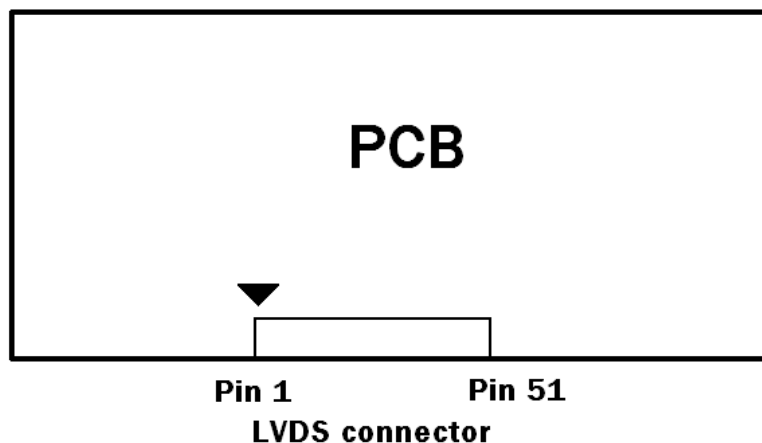
Note (11) Please reference Appendix A

Note (12) Currently, we only support line alternative format (1st line is left signal), show as the attached block diagram. In the future, we will support other format.



Line alternative format

Note (13) LVDS connector pin order defined as follows



5.2 BACKLIGHT UNIT

The pin configuration for the housing and leader wire is shown in the table below.

CN2,3,6,7: 196388-12041-3 (P-TWO)

Pin №	Symbol	Feature
1	VLED	Positive of LED String
2	VLED	
3	VLED	
4	VLED	
5	NC	NC
6	NC	
7	NC	
8	NC	
9	N1	Negative of LED String
10	N2	
11	N3	
12	N4	

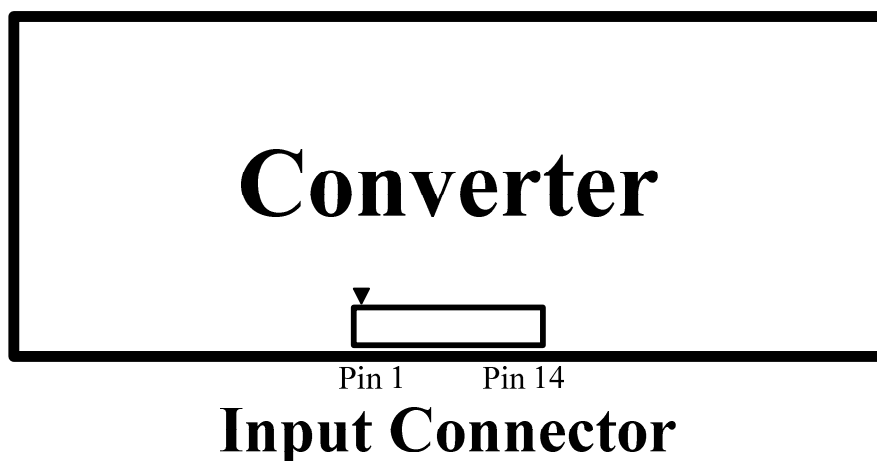
5.3 CONVERTER UNIT

CN1(Header): CI0114M1HR0-LA (CvilLux)

Pin No.	Symbol	Feature
1	VBL	+24V
2		
3		
4		
5		
6	GND	GND
7		
8		
9		
10		
11	ERR	Normal (GND) Abnormal (Open)
12	BLON	BL ON/OFF
13	NC	NC
14	E_PWM	External PWM Control

Note (1) If Pin14 is open, E_PWM is 100% duty.

Note (2) Input connector pin order defined as follows

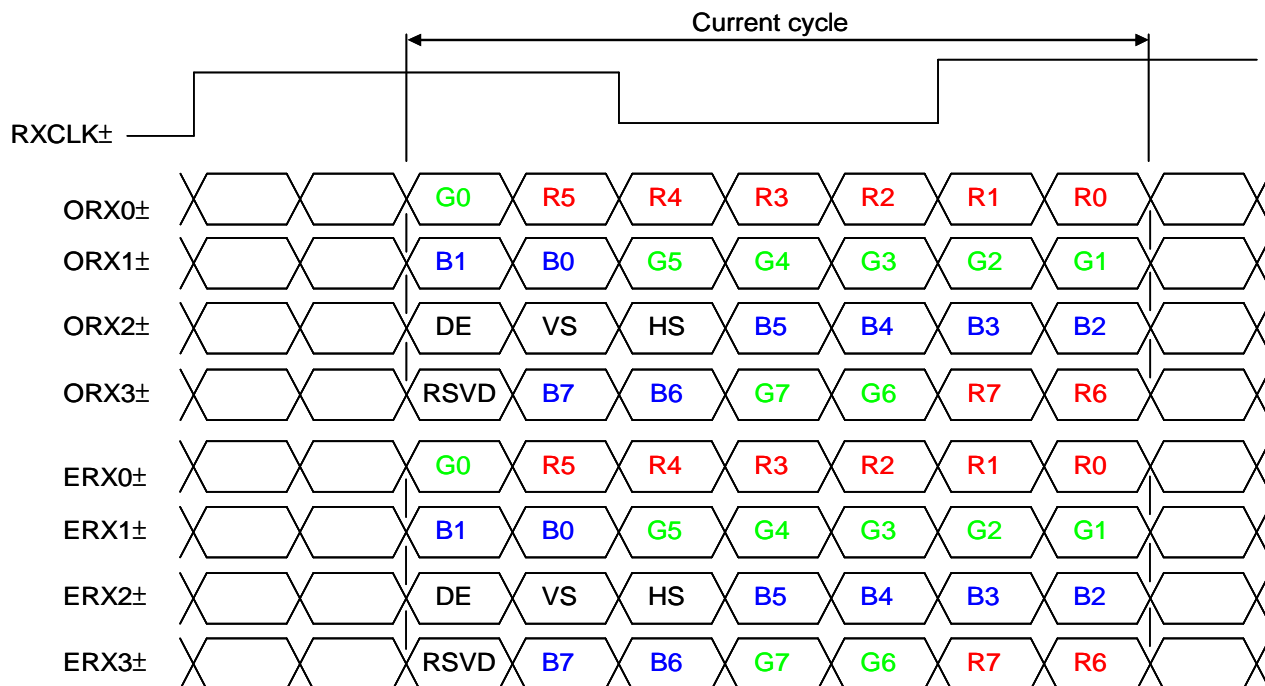


5.4 LVDS INTERFACE

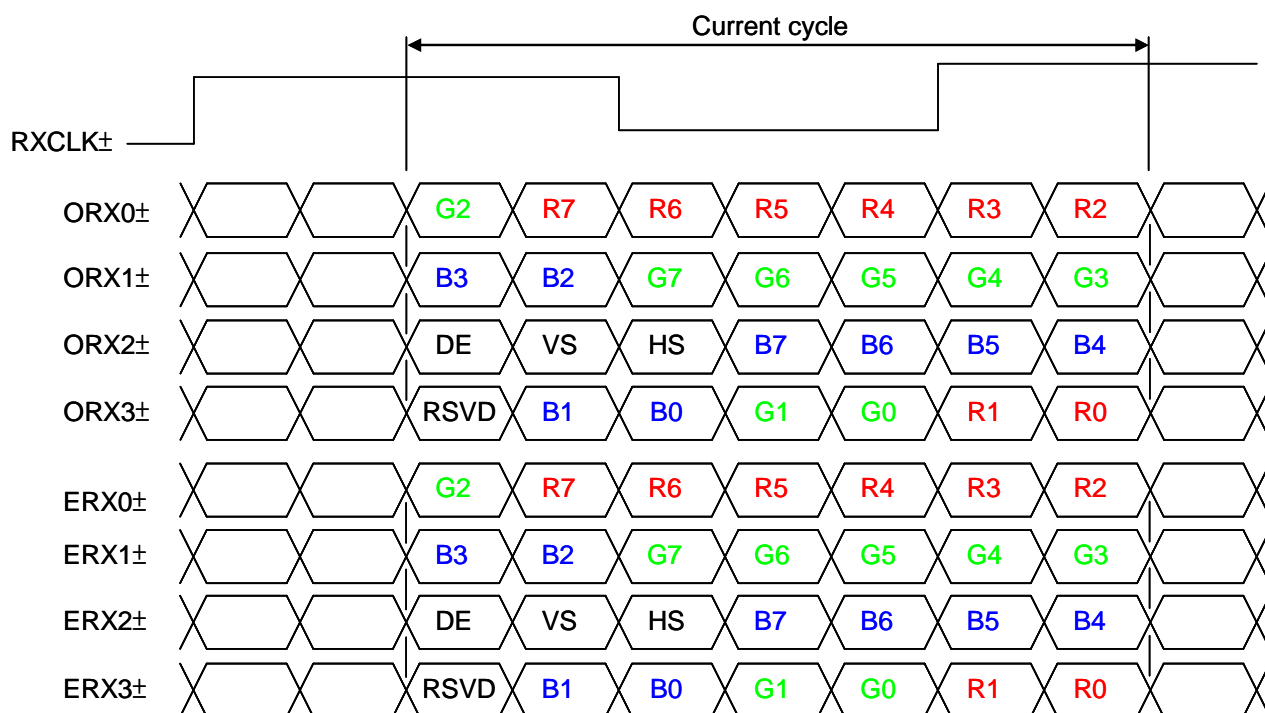
JEIDA Format : SELLVDS = L

VESA Format : SELLVDS = H or Open

VESA LVDS format



JEDIA LVDS format



5.5 COLOR DATA INPUT ASSIGNMENT

The brightness of each primary color (red, green and blue) is based on the 8-bit gray scale data input for the color. The higher the binary input, the brighter the color. The table below provides the assignment of the color versus data input.

Color		Data Signal																														
		Red								Green								Blue														
R7	R6	R5	R4	R3	R2	R1	R0	G7	G6	G5	G4	G3	G2	G1	G0	B7	B6	B5	B4	B3	B2	B1	B0									
Basic Colors	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
	Red	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
	Green	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
	Blue	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	
	Cyan	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	
	Magenta	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
	Yellow	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	White	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Gray Scale Of Red	Red (0) / Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red (1)	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red (2)	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Red (253)	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red (254)	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red (255)	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Gray Scale Of Green	Green (0) / Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Green (1)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Green (2)	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Green (253)	0	0	0	0	0	0	0	0	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Green (254)	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Green (255)	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Gray Scale Of Blue	Blue (0) / Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Blue (1)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
	Blue (2)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Blue (253)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	0	1	0	0
	Blue (254)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0
	Blue (255)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Note (1) 0: Low Level Voltage, 1: High Level Voltage

6. INTERFACE TIMING

6.1 INPUT SIGNAL TIMING SPECIFICATIONS

The input signal timing specifications are shown as the following table and timing diagram. ($T_a = 25 \pm 2^\circ\text{C}$)

Signal	Item	Symbol	Min.	Typ.	Max.	Unit	Note
LVDS Receiver Clock	Frequency	F_{clkin} (=1/TC)	60	74.25	77	MHz	
	Input cycle to cycle jitter	T_{rcl}	-	-	200	ps	(2)
	Spread spectrum modulation range	$F_{\text{clkin_mod}}$	$F_{\text{clkin}}-2\%$	-	$F_{\text{clkin}}+2\%$	MHz	(3)
	Spread spectrum modulation frequency	F_{SSM}	-	-	200	KHz	
LVDS Receiver Data	Receiver Skew Margin	T_{RSKM}	-400	-	400	ps	(4)

6.1.1 Timing spce for Frame Rate = 50Hz

Signal	Item		Symbol	Min.	Typ.	Max.	Unit	Note
Frame rate	2D mode		F_{r5}	47	50	53	Hz	(8),(9)
	3D mode		F_{r5}	50	50	50	Hz	(6),(8),(9)
Vertical Active Display Term	2D Mode	Total	T_v	1115	1125	1380	Th	$T_v=T_{vd}+T_{vb}$
		Display	T_{vd}	1080	1080	1080	Th	—
		Blank	T_{vb}	35	45	300	Th	—
	3D Mdoe	Total	T_v	1350			Th	(5), (7)
		Display	T_{vd}	1080			Th	
		Blank	T_{vb}	270			Th	
Horizontal Active Display Term	2D Mode	Total	T_h	1050	1100	1150	T_c	$T_h=T_{hd}+T_{hb}$
		Display	T_{hd}	960	960	960	T_c	—
		Blank	T_{hb}	90	140	190	T_c	—
	3D Mdoe	Total	T_h	1050	1100	1150	T_c	$T_h=T_{hd}+T_{hb}$
		Display	T_{hd}	960	960	960	T_c	—
		Blank	T_{hb}	90	140	190	T_c	—

6.1.2 Timing spec for Frame Rate = 60Hz

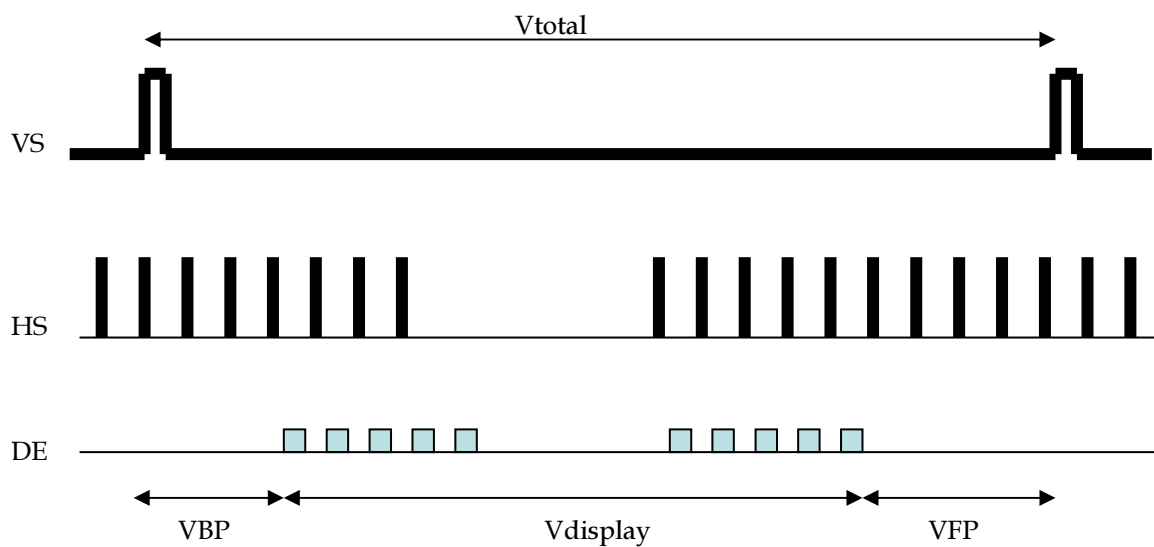
Signal	Item		Symbol	Min.	Typ.	Max.	Unit	Note
Frame rate	2D mode		F_{r6}	57	60	62.5	Hz	(8),(9)
	3D mode		F_{r6}	60	60	60	Hz	(6),(8),(9)
Vertical Active Display Term	2D Mode	Total	T_v	1115	1125	1380	Th	$T_v=T_{vd}+T_{vb}$
		Display	T_{vd}	1080	1080	1080	Th	—
		Blank	T_{vb}	35	45	300	Th	—
	3D Mdoe	Total	T_v	1125			Th	(5), (7)
		Display	T_{vd}	1080			Th	
		Blank	T_{vb}	45			Th	
Horizontal Active Display Term	2D Mode	Total	T_h	1050	1100	1150	T_c	$T_h=T_{hd}+T_{hb}$
		Display	T_{hd}	960	960	960	T_c	—
		Blank	T_{hb}	90	140	190	T_c	—
	3D Mdoe	Total	T_h	1050	1100	1150	T_c	$T_h=T_{hd}+T_{hb}$
		Display	T_{hd}	960	960	960	T_c	—
		Blank	T_{hb}	90	140	190	T_c	—

Note (1) Please make sure the range of pixel clock has follow the below equation:

$$F_{clk}(max) \geq F_{r6} \times T_v \times T_h$$

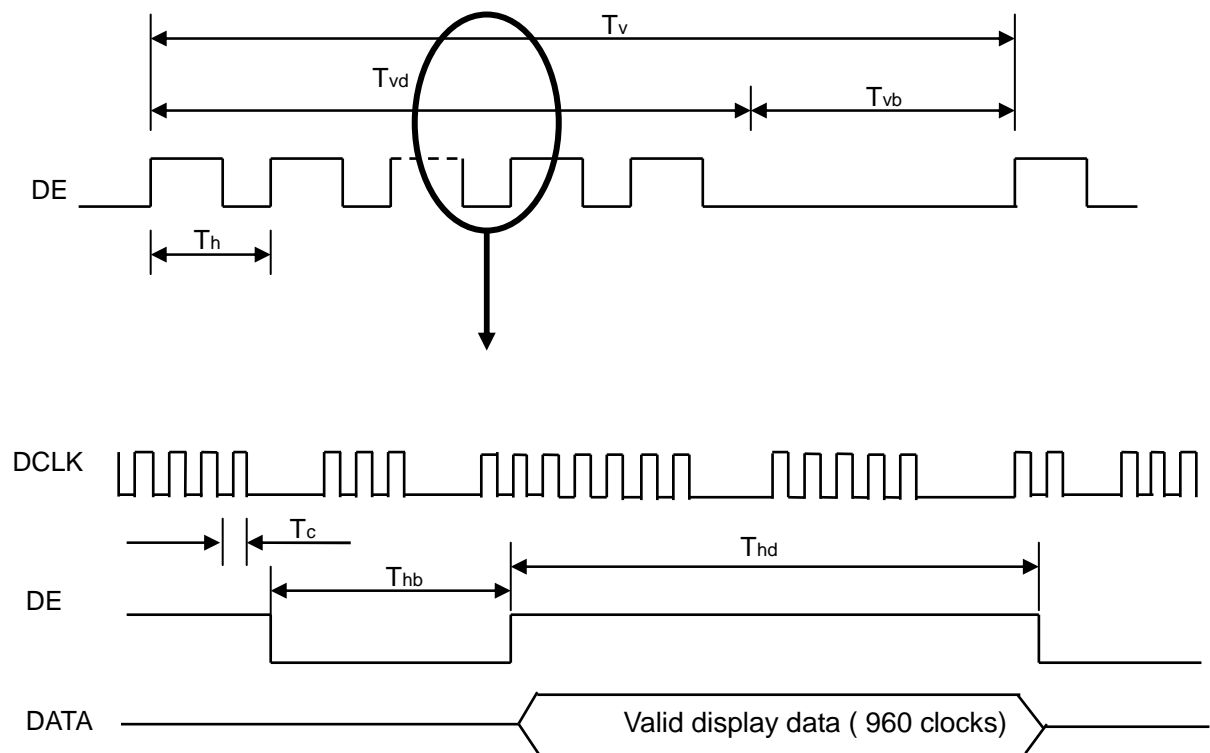
$$F_{r5} \times T_v \times T_h \geq F_{clk}(min)$$

INPUT SIGNAL TIMING DIAGRAM

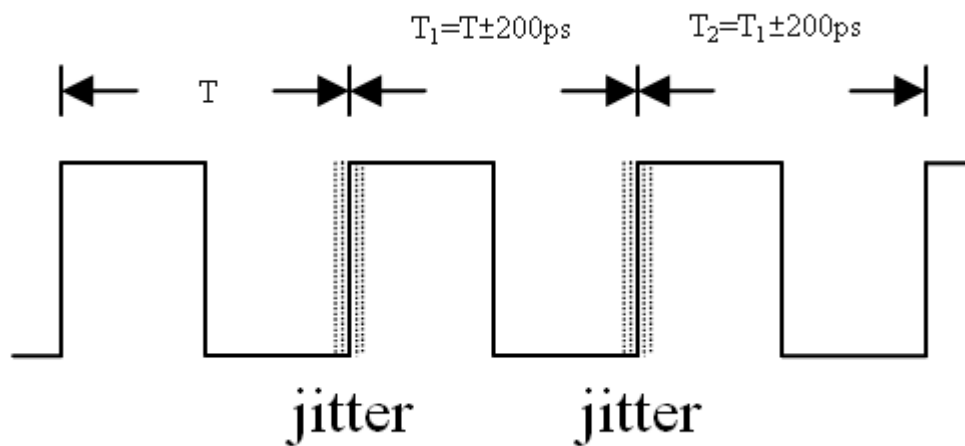


- VBP max : 150 line

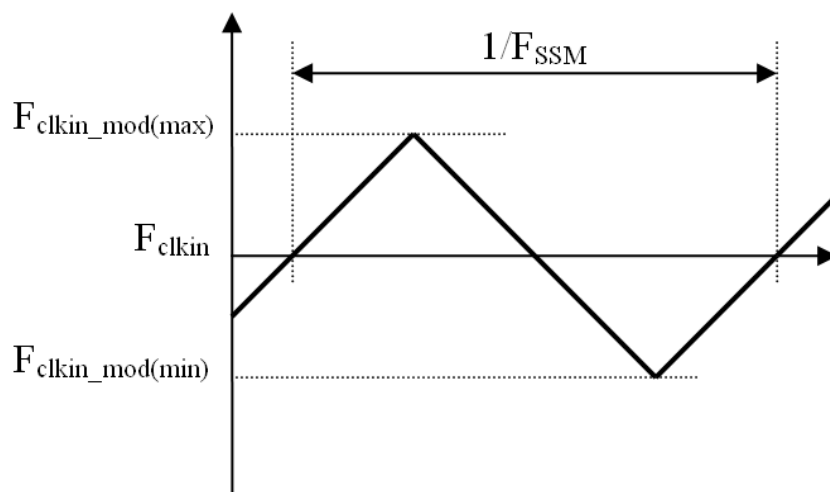
Suggest $VBP = VFP = \frac{1}{2} * (V_{total} - V_{display})$



Note (2) The input clock cycle-to-cycle jitter is defined as below figures. $Trcl = |T_1 - T_1|$

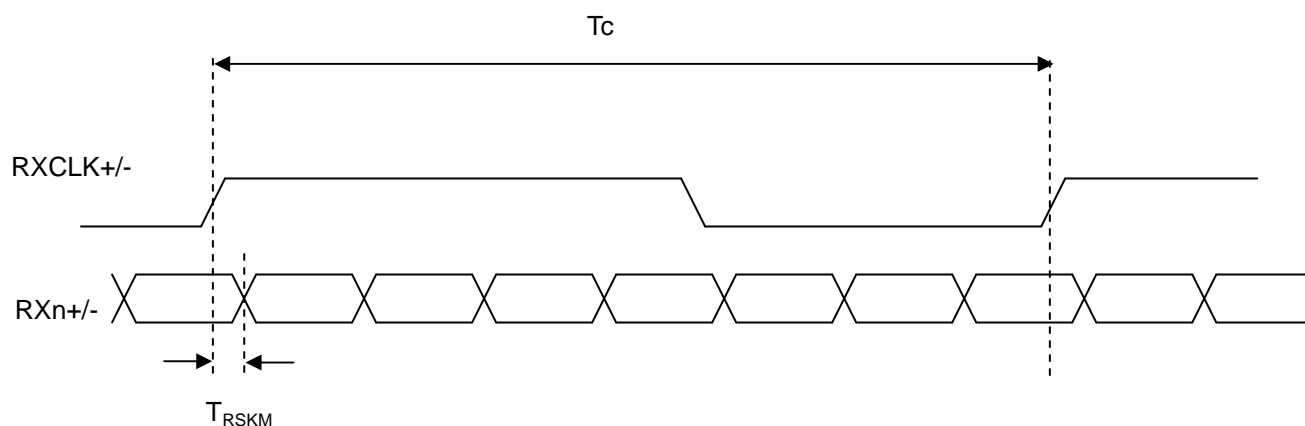


Note (3) The SSCG (Spread spectrum clock generator) is defined as below figures.



Note (4) LVDS receiver skew margin is defined and shown as below.

LVDS RECEIVER INTERFACE TIMING DIAGRAM



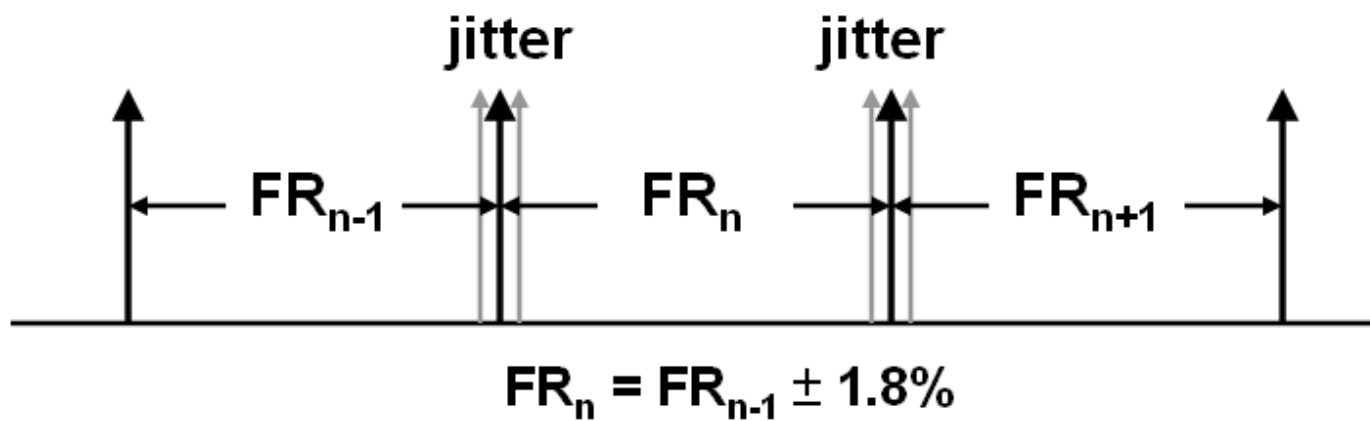
Note (5) Please fix the Vertical timing (Vertical Total =1350 / Display =1080 / Blank = 270) in 50Hz 3D mode
and Vertical timing (Vertical Total =1125 / Display =1080 / Blank = 45) in 60Hz 3D mode

Note (6) In 3D mode, the set up Fr5 and Fr6 in Typ. ± 3 Hz .In order to ensure that the electric function performance
to avoid no display symptom.(Except picture quality symptom.)

Note (7) In 3D mode, the set up Tv and Tvb in Typ. ± 30 .In order to ensure that the electric function performance to
avoid no display symptom.(Except picture quality symptom.)

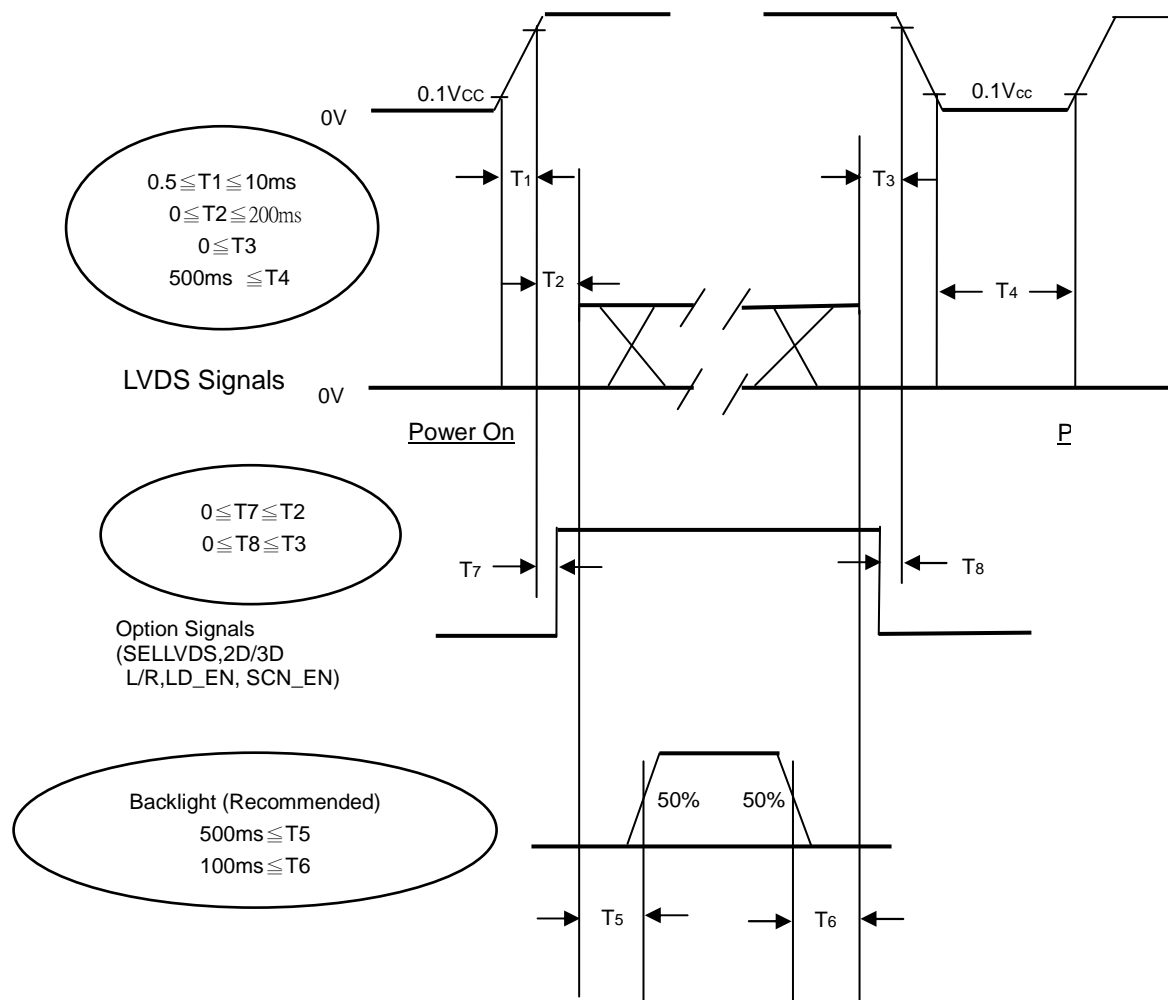
Note (8) The frame-to-frame jitter of the input frame rate is defined as the above figures. $FR_n = FR_{n-1} \pm 1.8\%$.

Note (9) The setup of the frame rate jitter $> 1.8\%$ may result in the cosmetic LED backlight symptom but the electric
function is not affected.

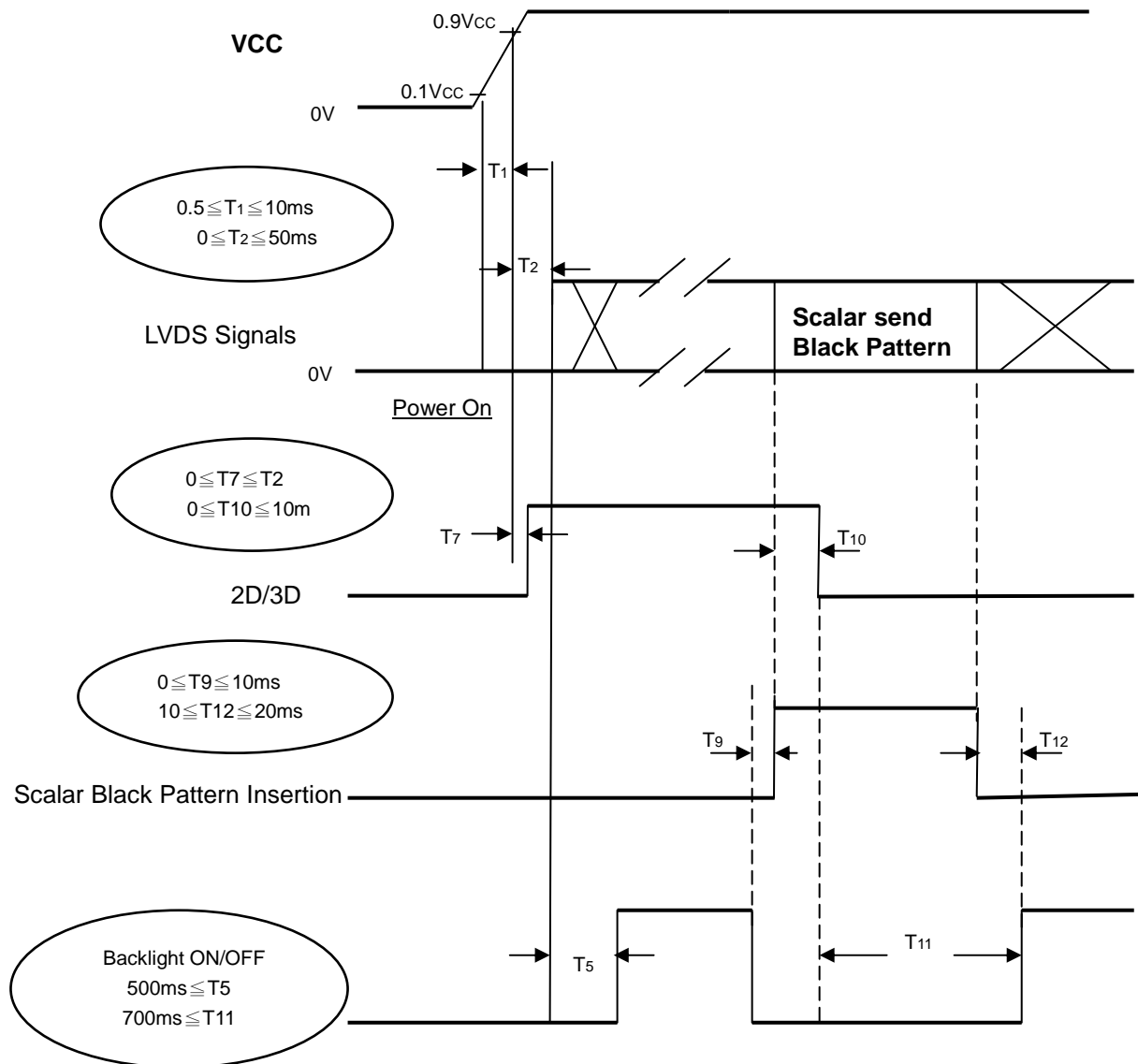


6.2 POWER ON/OFF SEQUENCE

To prevent a latch-up or DC operation of LCD module, the power on/off sequence should be as the diagram below.



6.3 2D/3D MODE CHANGE SIGNAL SEQUENCE WITHOUT VCC TURN OFF AND TURN ON



Note (1) The supply voltage of the external system for the module input should follow the definition of Vcc.

Note (2) Apply the LED voltage within the LCD operation range. When the backlight turns on before the LCD operation or the LCD turns off before the backlight turns off, the display may momentarily become abnormal screen.

Note (3) In case of Vcc is in off level, please keep the level of input signals on the low or high impedance. If $T_2 < 0$, that maybe cause electrical overstress failure.

Note (4) T4 should be measured after the module has been fully discharged between power off and on period.

Note (5) Interface signal shall not be kept at high impedance when the power is on.

Note (6) When 2D/3D mode is changed, TCON will insert black pattern internally. During black insertion, TCON would load required optical table and TCON parameter setting. The black insertion time should be longer than 650ms because TCON must recognize 2D or 3D format and set the correct parameter.

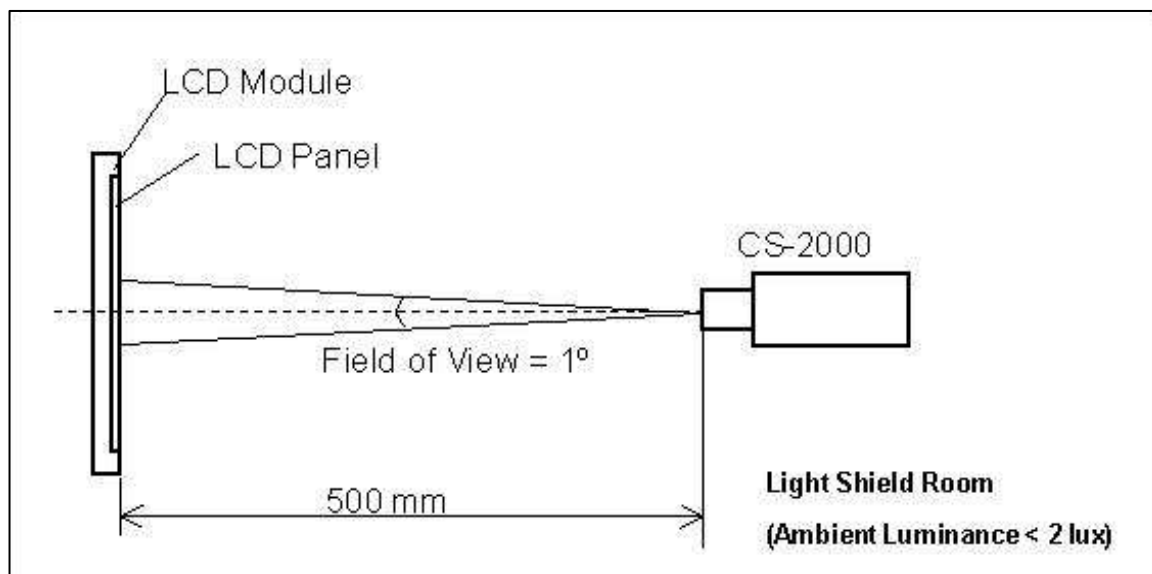
7. OPTICAL CHARACTERISTICS

7.1 TEST CONDITIONS

Item	Symbol	Value	Unit
Ambient Temperature	Ta	25±2	°C
Ambient Humidity	Ha	50±10	%RH
Supply Voltage	V _{CC}	12±1.2	V
Input Signal	According to typical value in "3. ELECTRICAL CHARACTERISTICS"		
LED Current	I _L	115±3.45	mA

The LCD module should be stabilized at given temperature for 1 hour to avoid abrupt temperature change during measuring in a windless room.

Local Dimming Function should be Disable before testing to get the steady optical characteristics (According to 5.1 CNF1 Connector Pin Assignment, Pin no. "42")



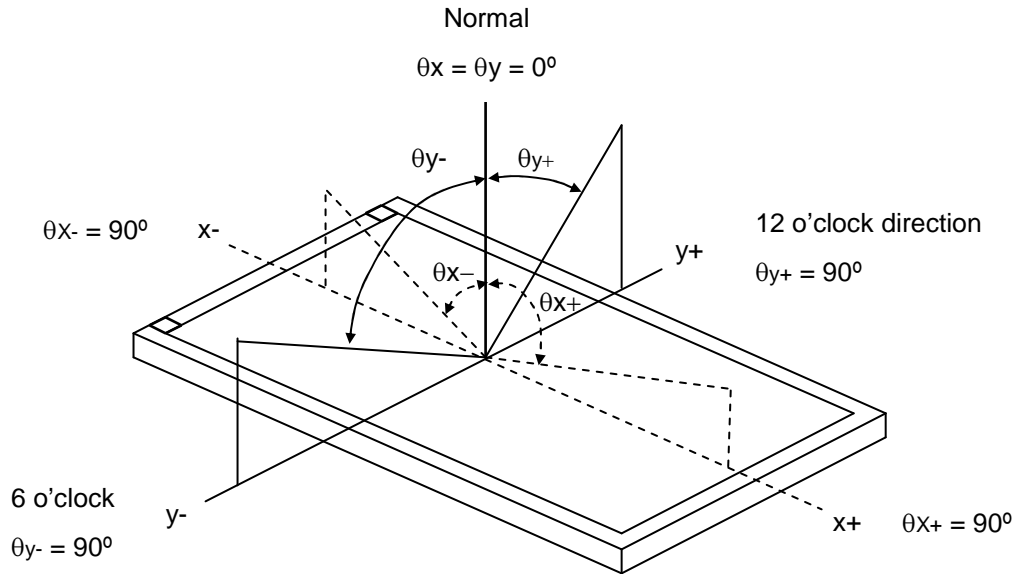
7.2 OPTICAL SPECIFICATIONS

The relative measurement methods of optical characteristics are shown in 7.2. The following items should be measured under the test conditions described in 7.1 and stable environment shown in 7.1.

Item		Symbol		Condition	Min.	Typ.	Max.	Unit	Note	
Contrast Ratio		CR		$\theta_x=0^\circ, \theta_Y=0^\circ$ Viewing angle at normal direction	3500	5000	-	-	Note (2)	
Response Time		Gray to gray				6.5	13	ms	Note (3)	
Center Luminance of White	L_C	2D			280	350	-	cd/m ²	Note (4)	
		3D				85	-	cd/m ²	Note (8)	
White Variation		δW					1.3	-	Note (6)	
Cross Talk	CT	2D			-		4	%	Note (5)	
		3D-W				4	-	%	Note (8)	
		3D-D				11	-	%	Note (8)	
Color Chromaticity	Red	Rx			Typ.- 0.03	0.644	Typ.+ 0.03	-		
		Ry						-		
	Green	Gx		0.330				-		
		Gy		0.296				-		
	Blue	Bx		0.595				-		
		By		0.148				-		
	White	Wx		0.054				-		
		Wy		0.280				-		
	Correlated color temperature							0.290		-
								9800		K
	Color Gamut	C.G.		-	72	-	%	NTSC		
Viewing Angle	Horizontal	θ_x+		CR≥20	80	88	-	Deg.	(1)	
		θ_x-			80	88	-			
	Vertical	θ_Y+			80	88	-			
		θ_Y-			80	88	-			
Transmission direction of the up polarizer		Φ_{up}		-	-	90	-	Deg.	(7)	

Note (1) Definition of Viewing Angle (θ_x , θ_y) :

Viewing angles are measured by Autronic Conoscope Cono-80.



Note (2) Definition of Contrast Ratio (CR) :

The contrast ratio can be calculated by the following expression.

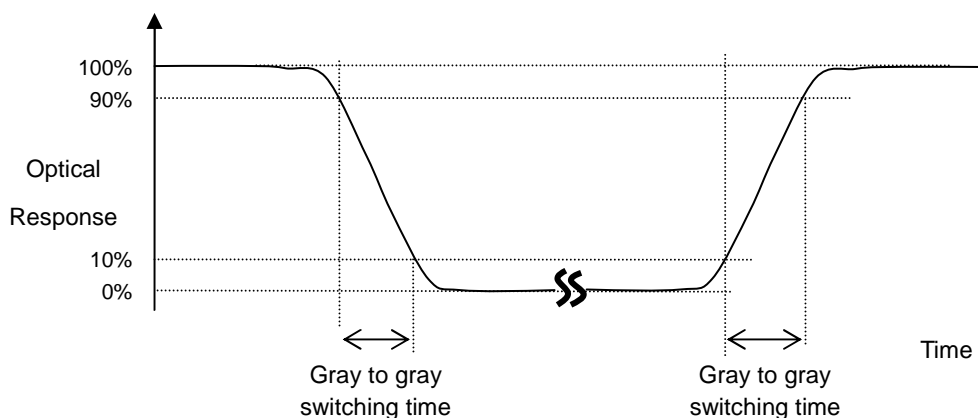
$$\text{Contrast Ratio (CR)} = \frac{\text{Surface Luminance of L1023}}{\text{Surface Luminance of L0}}$$

L1023: Luminance of gray level 1023

L 0: Luminance of gray level 0

CR = CR (5), where CR (X) is corresponding to the Contrast Ratio of the point X at the figure in Note (6).

Note (3) Definition of Gray-to-Gray Switching Time :



The driving signal means the signal of gray level 0, 124, 252, 380, 508, 636, 764, 892 and 1023.

Gray to gray average time means the average switching time of gray level 0, 124, 252, 380, 508, 636, 764, 892 and 1023 to each other.

Note (4) Definition of Luminance of White (L_C) :

Measure the luminance of gray level 1023 at center point.

$L_C = L(5)$, where $L(x)$ is corresponding to the luminance of the point X at the figure in Note (6).

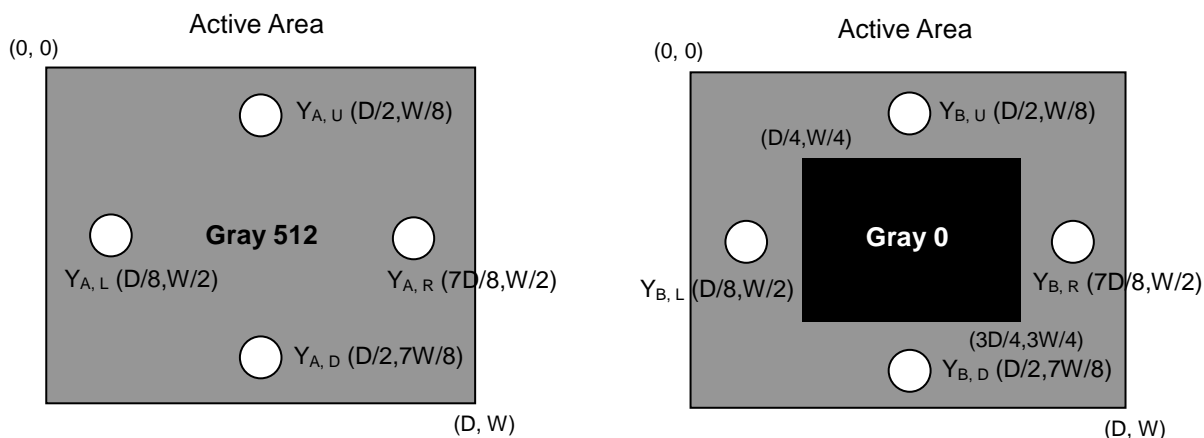
Note (5) Definition of Cross Talk (CT) :

$$CT = |Y_B - Y_A| / Y_A \times 100 (\%)$$

Where:

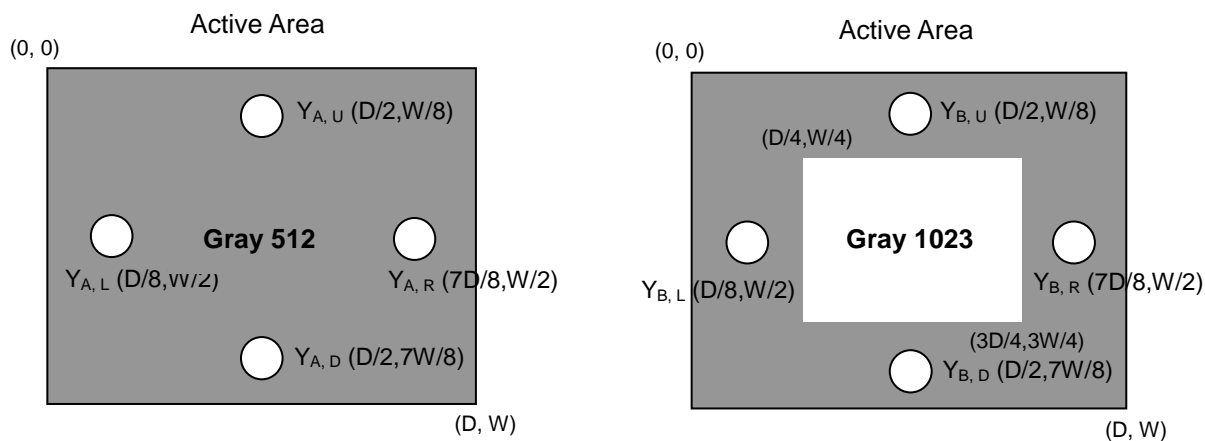
Y_A = Luminance of measured location without gray level 0 pattern (cd/m²)

Y_B = Luminance of measured location with gray level 0 pattern (cd/m²)



Y_A = Luminance of measured location without gray level 1023 pattern (cd/m²)

Y_B = Luminance of measured location with gray level 1023 pattern (cd/m²)



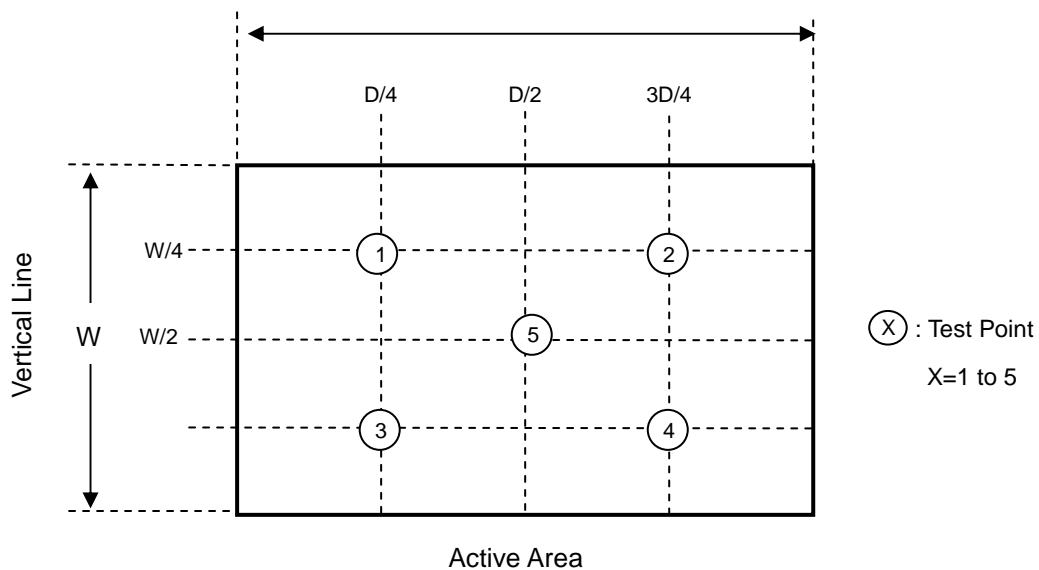
Note (6) Definition of White Variation (δW):

Measure the luminance of gray level 1023 at 5 points

$$\delta W = \text{Maximum} [L(1), L(2), L(3), L(4), L(5)] / \text{Minimum} [L(1), L(2), L(3), L(4), L(5)]$$

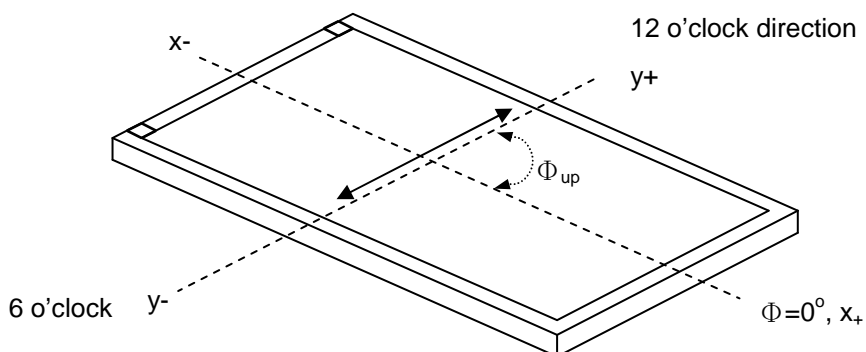
Horizontal Line

D



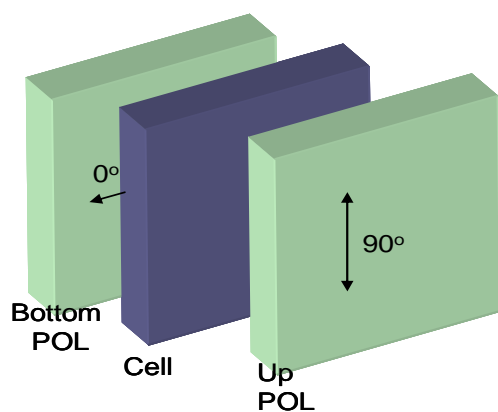
Note (7) This is a reference for designing the shutter glasses of 3D application.

Definition of the transmission direction of the up polarizer:

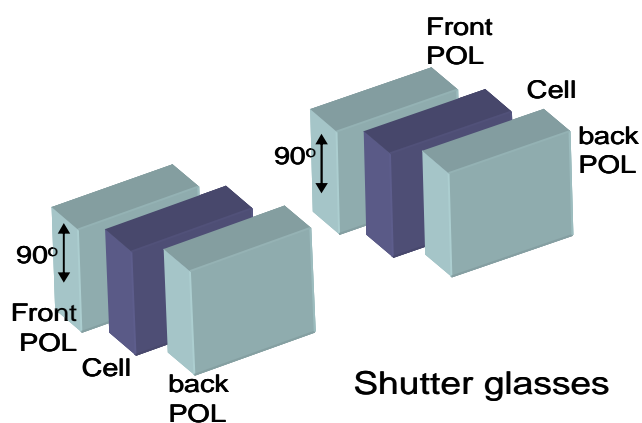


The transmission axis of the front polarizer of the shutter glasses should be parallel to this panel transmission

direction to get a maximum 3D mode luminance.



LCD module




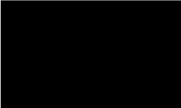


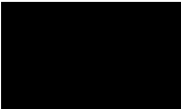
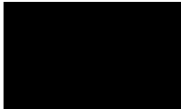


Shutter glasses

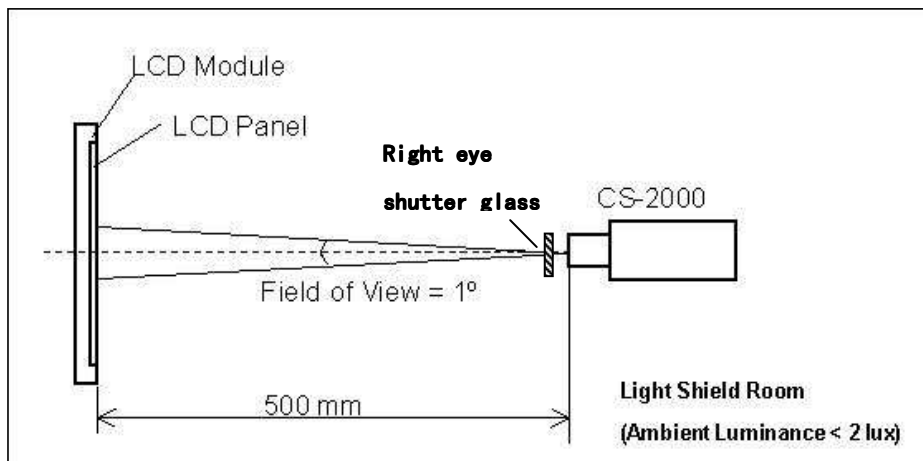
Note (8) Definition of the 3D mode performance (measured under 3D mode, use CMI's shutter glass):

a. Test pattern

Left eye image and right eye image are displayed alternated

		WW Left eye image: W1023; Right eye image: W1023
		WB Left eye image: W1023; Right eye image: W0
		BW Left eye image: W0; Right eye image: W1023
		BB Left eye image: W0; Right eye image: W0

b. Measurement setup



Shutter glasses are well controlled under suitable timing, and measure the luminance of the center point of the panel through the right eye glass. The transmittance of the glass should be larger than 40.0% under 3D mode operation.

The luminance of the test pattern "WW", denoted $L(WW)$; the luminance of the test pattern "WB", denoted $L(WB)$; the luminance of the test pattern "BW", denoted $L(BW)$; the luminance of the test pattern "BB", denoted $L(BB)$

c. Definition of the Center Luminance of White, L_c (3D) : $L(WW)$

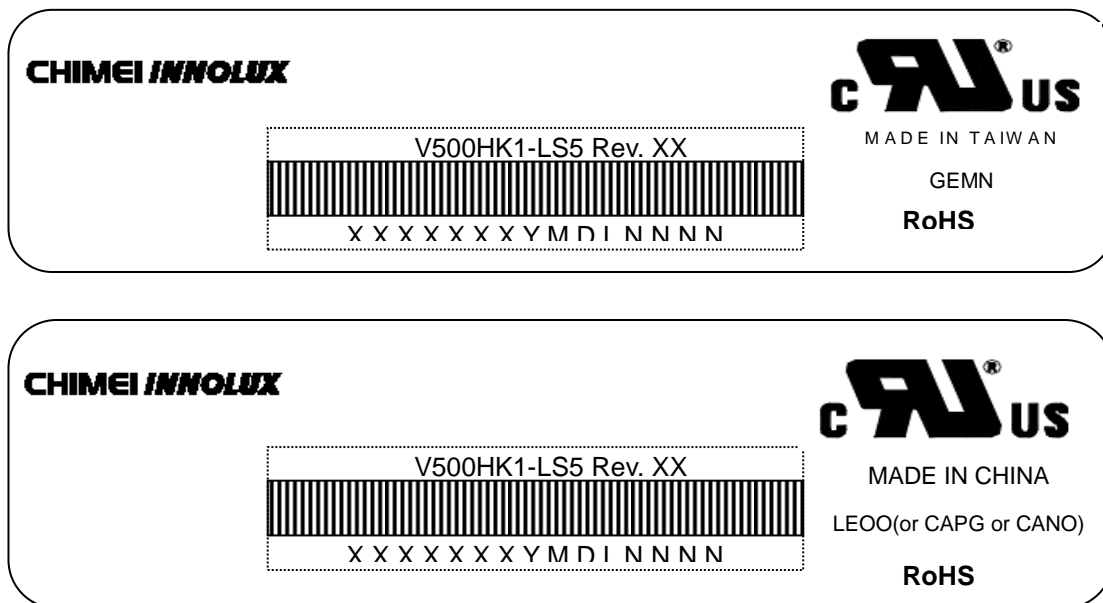
d. Definition of the 3D mode white crosstalk, CT (3D-W) : $CT(3D-W) \equiv \frac{L(WB) - L(BB)}{L(WW) - L(BB)}$

e. Definition of the 3D mode dark crosstalk, CT (3D-D) : $CT(3D-D) \equiv \frac{L(WW) - L(BW)}{L(WW) - L(BB)}$

8. DEFINITION OF LABELS

8.1 CMI MODULE LABEL

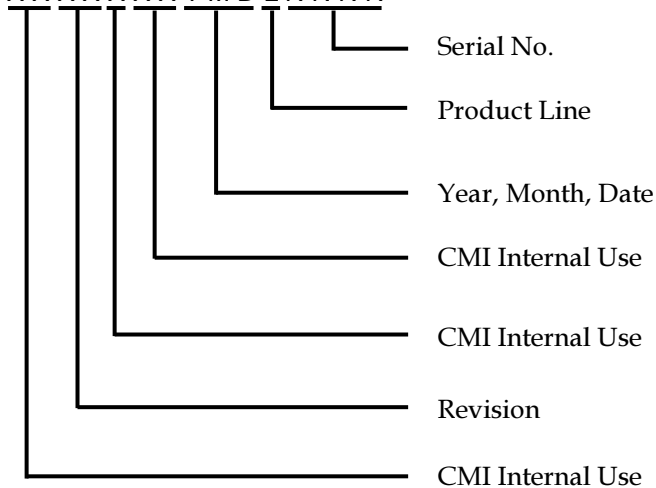
The barcode nameplate is pasted on each module as illustration, and its definitions are as following explanation.



Model Name: V500HK1-LS5

Revision: Rev. XX, for example: A0, A1... B1, B2... or C1, C2...etc.

Serial ID: X X X X X X Y M D L N N N N



Serial ID includes the information as below:

Manufactured Date:

Year : 2001=1, 2002=2, 2003=3, 2004=4...2010=0, 2011=1, 2012=2...

Month: 1~9, A~C, for Jan. ~ Dec.

Day: 1~9, A~Y, for 1st to 31st, exclude I ,O, and U.

Revision Code : Cover all the change

Serial No. : Manufacturing sequence of product

Product Line : 1 → Line1, 2 → Line 2, ...etc.

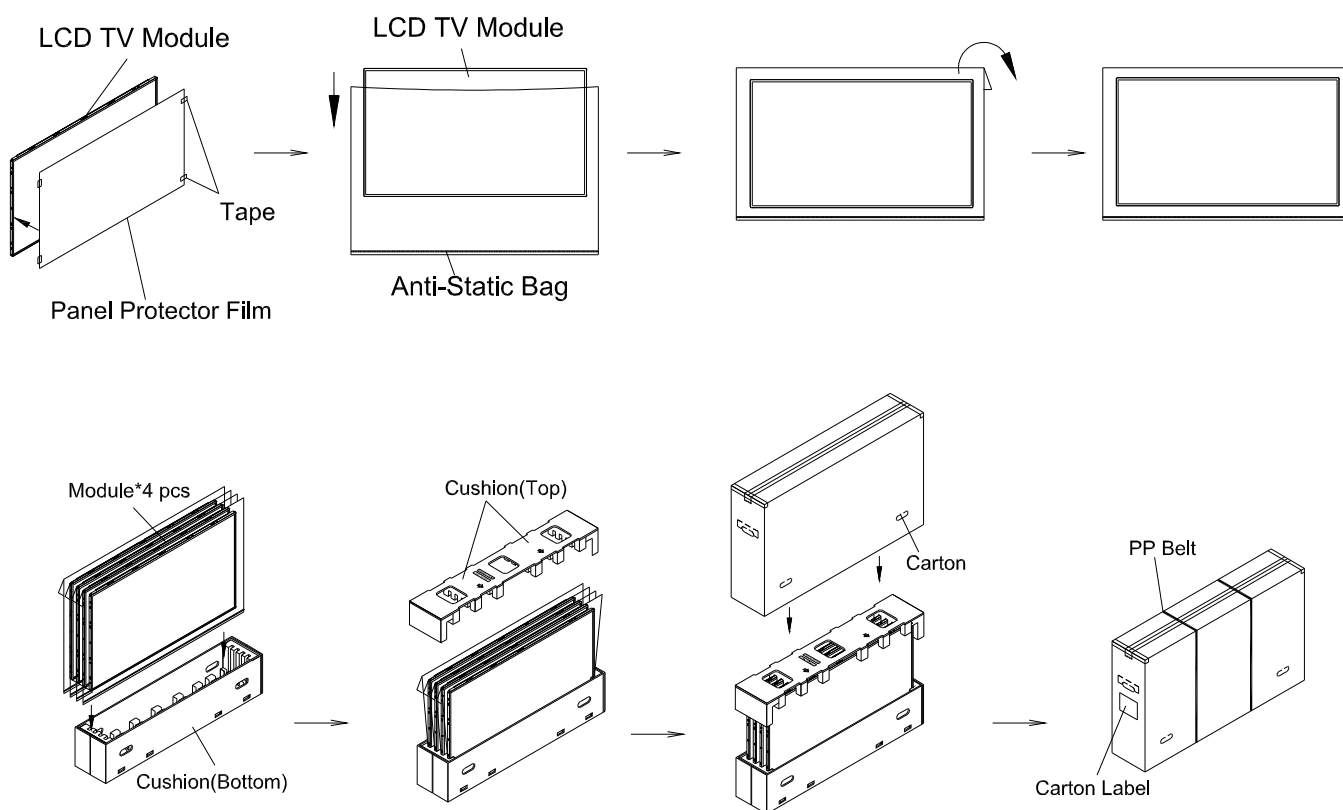
9. PACKAGING

9.1 PACKAGING SPECIFICATIONS

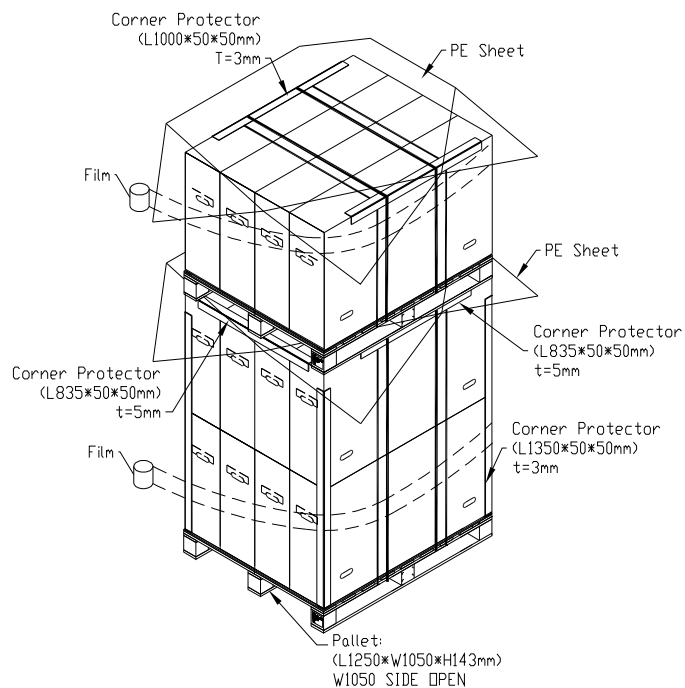
- (1) 4 LCD TV modules / 1 Box
- (2) Box dimensions: 1235(L) X 258 (W) X 751 (H)
- (3) Weight: approximately 59.8 Kg (4 modules per box)

9.2 PACKAGING METHOD

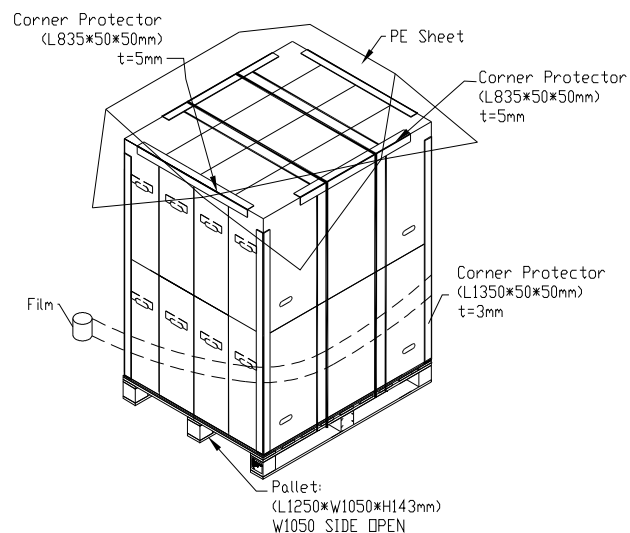
Packaging method is shown in following figures.



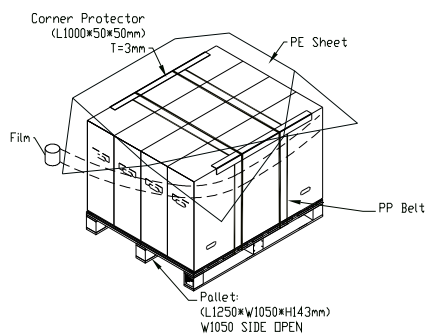
Sea / Land Transportation (40ft HQ Container)



Sea / Land Transportation (40ft Container)



Air Transportation



10. PRECAUTIONS

10.1 ASSEMBLY AND HANDLING PRECAUTIONS

- (1) Do not apply rough force such as bending or twisting to the module during assembly.
- (2) It is recommended to assemble or to install a module into the user's system in clean working areas. The dust and oil may cause electrical short or worsen the polarizer.
- (3) Do not apply pressure or impulse to the module to prevent the damage of LCD panel and backlight.
- (4) Always follow the correct power-on sequence when the LCD module is turned on. This can prevent the damage and latch-up of the CMOS LSI chips.
- (5) Do not plug in or pull out the I/F connector while the module is in operation.
- (6) Do not disassemble the module.
- (7) Use a soft dry cloth without chemicals for cleaning, because the surface of polarizer is very soft and easily scratched.
- (8) Moisture can easily penetrate into LCD module and may cause the damage during operation.
- (9) High temperature or humidity may deteriorate the performance of LCD module. Please store LCD modules in the specified storage conditions.
- (10) When ambient temperature is lower than 10°C, the display quality might be reduced. For example, the response time will become slow, and the starting voltage of LED will be higher than that of room temperature.

10.2 SAFETY PRECAUTIONS

- (1) The startup voltage of a backlight is over 1000 Volts. It may cause an electrical shock while assembling with the inverter. Do not disassemble the module or insert anything into the backlight unit.
- (2) If the liquid crystal material leaks from the panel, it should be kept away from the eyes or mouth. In case of contact with hands, skin or clothes, it has to be washed away thoroughly with soap.
- (3) After the module's end of life, it is not harmful in case of normal operation and storage.

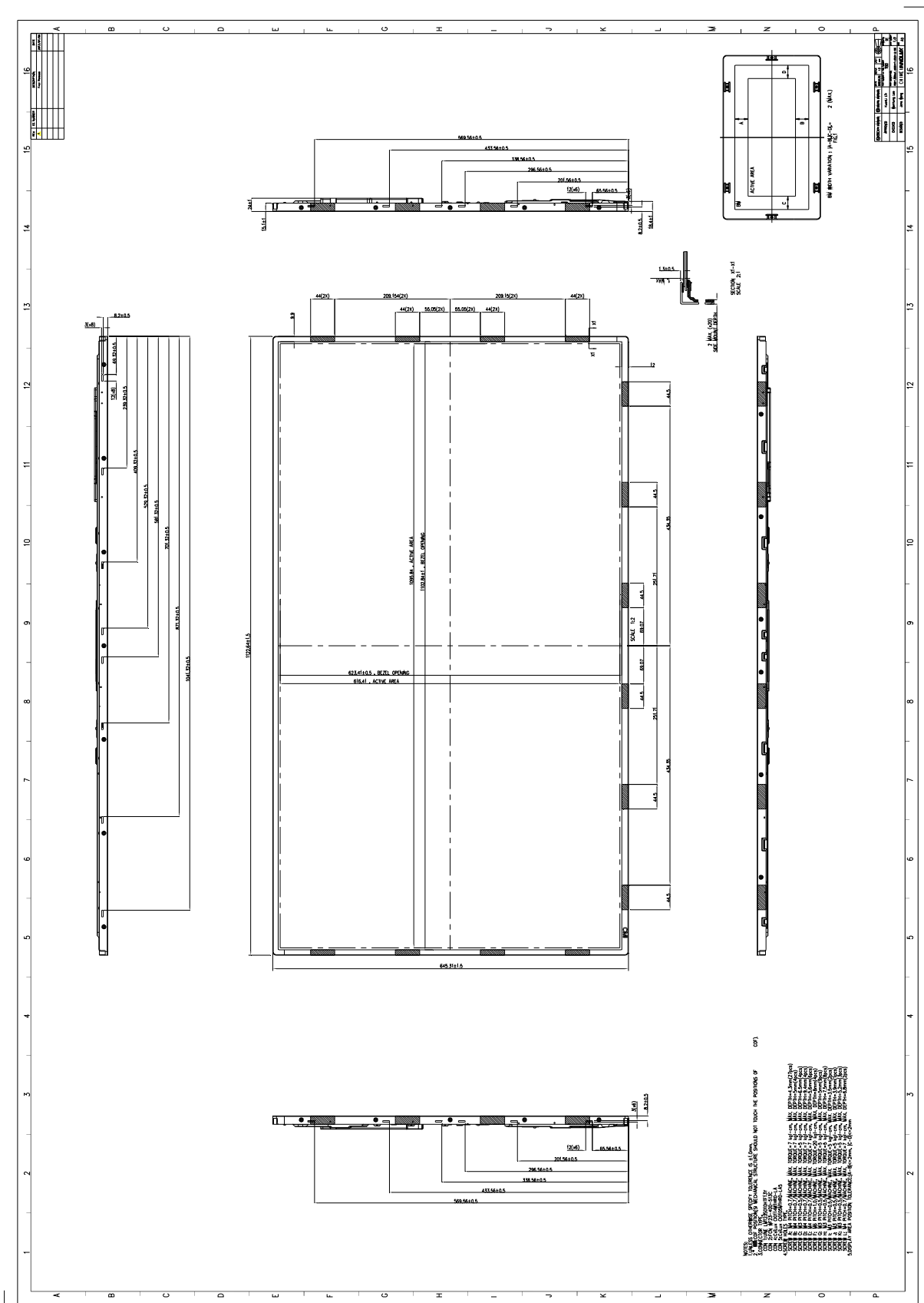
10.3 SAFETY STANDARDS

The LCD module should be certified with safety regulations as follows:

Regulatory	Item	Standard
Information Technology equipment	UL	UL60950-1:2006 or Ed.2:2007
	cUL	CAN/CSA C22.2 No.60950-1-03 or 60950-1-07
	CB	IEC60950-1:2005 / EN60950-1:2006+ A11:2009
Audio/Video Apparatus	UL	UL60065 Ed.7:2007
	cUL	CAN/CSA C22.2 No.60065-03:2006 + A1:2006
	CB	IEC60065:2001+ A1:2005 / EN60065:2002 + A1:2006+ A11:2008

If the module displays the same pattern for a long period of time, the phenomenon of image sticking may be occurred.

11. MECHANICAL CHARACTERISTIC





Appendix A

Local Dimming demo function

A.1 I2C address and write command

Device address: 0xe0

Register address: 0x65

Command data: 0x16 0x00 0x00 0x00 0x00 0x00: Local Dimming demo mode OFF (Note 1)

0x16 0x00 0x00 0x00 0x00 0x01 : Local Dimming demo mode ON (Demo in right half screen) (Note 2)

Preamble data: 0x26 0x38

I2C data:

	Device Address		Preamble data		Preamble data	
START	11100000 (0xE0)	ACK	00100110 (0x26)	ACK	00111000 (0x38)	ACK

Register Address		Command Data		Command Data	
01100101 (0x65)	ACK	00010110 (0x16)	ACK	00000000 (0x00)	ACK

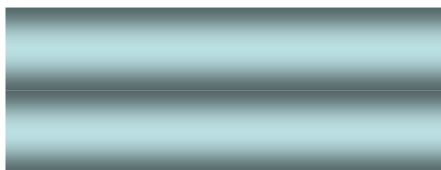
Command Data		Command Data		Command Data	
00000000 (0x00)	ACK	00000000 (0x00)	ACK	00000000 (0x00)	ACK

Command Data	
00000001 (0x01)	STOP

Note 1: Local Dimming demo OFF



Note 2: Local Dimming demo ON



A.2 I2C timing

Symbol	Parameter	Min.	Max.	Unit
t_{SU-STA}	Start setup time	250	-	ns
t_{HD-STA}	Start hold time	250	-	ns
t_{SU-DAT}	Data setup time	80	-	ns
t_{HD-DAT}	Data hold time	0	-	ns
t_{SU-STO}	Stop setup time	250	-	ns
t_{BUF}	Time between Stop condition and next Start condition	500	-	ns

